APPENDIX E

AVAILABLE TRANSDUCER DOCUMENTATION

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APPENDIX F

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATION

APPENDIX F

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATION

1.0 General

The Continuously Variable Slope Delta (CVSD) modulation is a nonlinear, sampled data, feedback system which accepts a band-limited analog signal and encodes it into binary form for transmission through a digital channel. At the receiver, the binary signal is decoded into a close approximation of the original analog signal. A typical CVSD converter consisting of an encoder and decoder is shown in figures F-1a and b.

2.0 General Descriptions

A general description of the delta modulation and the CVSD converter can be found in the succeeding subparagraphs.

2.1 Delta Modulation. Delta modulation is an A-D conversion technique resulting in a form of digital pulse modulation. A delta modulator periodically samples the amplitude of a band-limited analog signal, and the amplitude differences of two adjacent samples are coded into n-bit code words. This nonlinear, sampled-data, feedback system then transmits the encoded bit stream through a digital channel. At the receiving end, an integrating network converts the delta-modulated bit stream through a decoding process into a close approximation of the original analog signal.

2.2 CVSD Converter. A typical CVSD converter consists of an encoder and a decoder (see figures F-1a and b). The analog input signal of the CVSD encoder is band-limited by the input band, pass filter. The CVSD encoder compares the band-limited analog input signal with an analog feedback approximation signal generated at the reconstruction integrator output. The digital output signal of the encoder is the output of the first register in the "run-of-three" counter. The digital output signal is transmitted at the clock (sample) rate and will equal "1" if the analog input signal is greater than or equal to the analog feedback signal at the instant of sampling. For this value of the digital output signal, the pulse amplitude modulator (PAM) applies a positive feedback pulse to the reconstruction integrator; otherwise, a negative pulse is applied. This function is accomplished by the polarity control signal, which is equal to the digital encoder output signal. The amplitude of the feedback pulse is derived by means of a 3-bit shift register, logic sensing for overload, and a syllabic lowpass filter. When a string of three consecutive ONES or ZEROS appears at the digital output, a discrete voltage level is applied to the syllabic filter, and the positive feedback pulse amplitude increases until the overload string is broken. In such an event, ground potential is fed to the filter by the overload algorithm, forcing a decrease in the amplitude of the slope voltage out of the syllabic filter. The encoder and decoder have identical characteristics

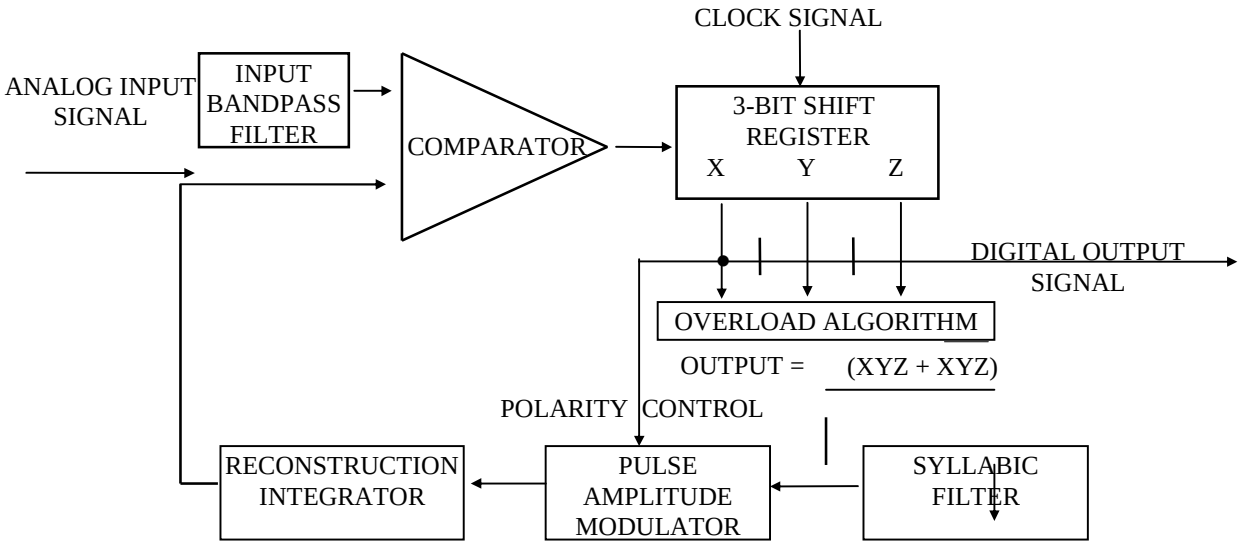

Figure F-1a. Typical CVSD encoder.

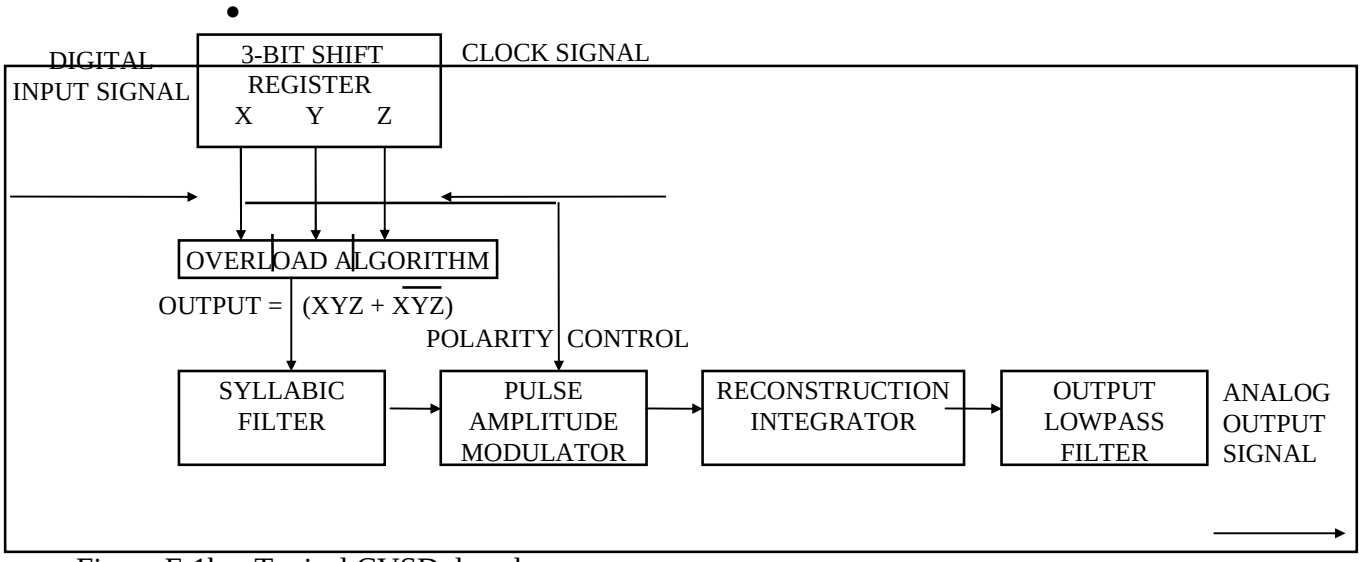

Figure F-1b. Typical CVSD decoder.

except for the comparator and filter functions. The CVSD decoder consists of the input band pass filter, shift register, overload algorithm, syllabic filter, PAM and reconstruction integrator used in the encoder, and an output low-pass filter. The decoder performs the inverse function of the encoder and regenerates speech by passing the analog output signal of the reconstruction integrator through the low-pass filter. Other characteristics optimize the CVSD modulation technique for voice signals. These characteristics include:

a. Changes in the slope of the analog input signal determine the step-size changes of the digital output signal.

b. The feedback loop is adaptive to the extent that the loop provides continuous or smoothly incremental changes in step size.

c. Companding is performed at a syllabic rate to extend the dynamic range of the analog input signal.

d. The reconstruction integrator is of the exponential (leaky) type to reduce the effects of digital errors.

3.0 Detailed Descriptions

The characteristics described in subparagraphs 3.1 through 3.9 are in addition to those specified in paragraph 5.0 of this standard and are for guidance only.

3.1 Input Band Pass Filter. The input filter provides band-limiting and is typically a second- or higher-order filter (see figure F-1a).

3.2 Comparator. The comparator compares the band-limited analog input signal from the filter with the output signal of the reconstruction integrator (see figure F-1a). This comparison produces the digital error signal input to the 3-bit shift register. The transfer characteristic of the comparator is such that the difference between the two input signals causes the output signal to be driven to saturation in the direction of the sign of the difference.

3.3 3-Bit Shift Register. The 3-bit shift register acts as a sampler which clocks the digital error signal from the comparator at the specified data signaling rate and stores the current samples and two previous samples of the error signal (see figures F-1a and b). The digital output signal is a binary signal having the same polarity as the input signal from the comparator at the time of the clock signal. The digital output signal is also the digital output of the encoder and is referred to as the baseband signal. Further processing for transmission such as conditioned diphase modulation may be applied to the baseband signal. It is necessary that the inverse of any such processing be accomplished and the baseband signal restored before the CVSD decoding process is attempted.

3.4 Overload Algorithm. The overload algorithm operates on the output of the 3-bit shift register (X, Y, Z) using the run-of-threes coincidence algorithm so that the algorithm output equals ($XYZ + \overline{XYZ}$) (see figures F-1a and b). The output signal is a binary signal at the clock signaling rate and is true for one clock period following the detection of three like bits and false at all other times.

3.5 Syllabic Filter. The syllabic filter acts as a low-pass filter for the output signal from the overload algorithm (see figures F-1a and b). The slope- voltage output of the syllabic filter is the modulating input to the PAM. The step-function response of the syllabic filter is related to the syllabic rate of speech, is independent of the sampling rate, and is exponential in nature. When the overload algorithm output is true, a charging curve is applicable. When this output is false, a discharging curve is applicable.

3.6 Pulse Amplitude Modulator (PAM). The PAM operates with two input signals: the output signal from the syllabic filter, and the digital signal from the 3-bit shift register (see figures F-1a and b). The syllabic filter output signal determines the amplitude of the PAM output signal and the signal from the 3-bit shift register is the polarity control that determines the direction, plus or minus, of the PAM output signal. The phrase "continuously variable" in CVSD is derived from the way the PAM output signal varies almost continuously.

3.7 Reconstruction Integrator. The reconstruction integrator operates on the output signal of the PAM to produce an analog feedback signal to the comparator (or an output signal to the output low-pass filter in the receiver) that is an approximation of the analog input signal (see figures F-1a and b).

3.8 Output Low-Pass Filter. The output filter is a low-pass filter having a frequency response that typically has an asymptotic rolloff with a minimum slope of 40 dB per octave, and a stopband rejection that is 45 dB or greater (see figure F-1b). The same output filter characteristic is used for encoder digital output signals of either 16 or 32 kbps.

3.9 Typical CVSD Decoder Output Envelope Characteristics. For a resistance/ capacitance circuit in the syllabic filter with time constants of 5 ms for both charging and discharging, the envelope characteristics of the signal at the decoder output are shown in figure F-2. For the case of switching the signal at the decoder input from the 0-percent run-of-threes digital pattern to the 30-percent run-of-threes digital pattern, the characteristic of the decoder output signal follows the resistance/ capacitance charge curve. Note that the number of time constants required to reach the 90-percent charge point is 2.3, which gives a nominal charge time of 11.5 ms.

When switching the other way (from the 30-percent pattern to the 0-percent pattern), the amplitude at the beginning of discharging is, at the first moment of switching, higher (by a factor of 16) than the final value which is reached asymptotically. The final value equals -24 dBm0, that is, 0.03. Therefore, the amplitude at the beginning of discharging is 0.48 (percent run-of-threes = 0). Note that the number of time constants required to reach the 10-percent point on the discharge curve is 1.57, which gives a nominal discharge time of 7.8 ms.

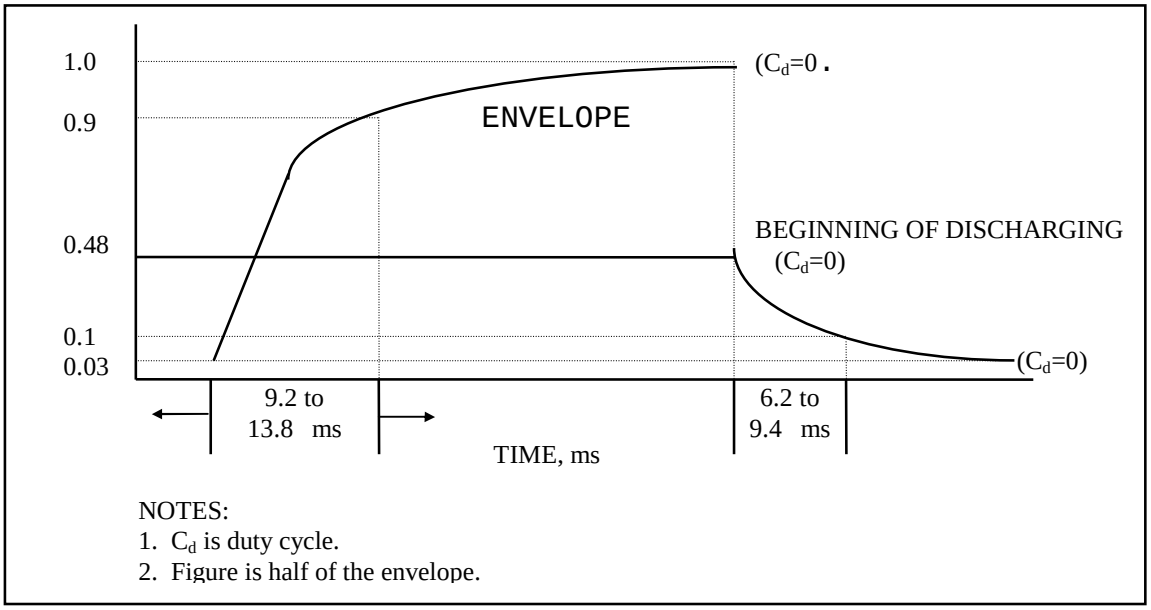

Figure F-2. Typical envelope characteristics of the decoder output signal for CVSD.

4.0 Reference Level

The decoder analog output level with the 16 and 32 kbps, 30-percent run-of-threes reference digital pattern applied to the decoder input shall be the reference level for the CVSD requirements of this standard, and shall be designated 0 dBm0 (see subparagraph 5.9.1).

5.0 CVSD Characteristics

The characteristics of CVSD are described in the following subparagraphs.

5.1 Input and Output Impedances. The analog input and output impedances for CVSD converters are not standardized. These impedances depend upon the application of the converters.

5.2 Data Signaling Rates. The CVSD converter shall be capable of operating at 16 and 32 kbps.

5.3 Input and Output Filters. The analog input shall be band pass filtered. The analog output shall be low pass filtered.

Details of input and output filers, consistent with the CVSD performance requirements of this standard, will be determined in applicable equipment specifications based on validated requirements.

5.4 Overload Algorithm. A 3-bit shift register shall be used for the CVSD encoder and decoder (see figures F-1a and b). The overload logic shall operate on the output of this shift register using the run-of-threes coincidence algorithm. The algorithm output signal shall be a binary signal at the data-signaling rate. This signal shall be true for one clock period following the detection of three like bits (all ZEROS or all ONES) and false at all other times.

5.5 Compression Ratio. The compression ratio shall be nominally 16:1 with a maximum of 21:1 and a minimum of 12:1. The maximum slope voltage shall be measured at the output of the syllabic filter for a 30-percent run-of-threes digital pattern. The minimum slope voltage shall be measured at the output of the syllabic filter for a 0-percent run-of--threes digital pattern.

5.6 Syllabic Filter. The syllabic filter shall have a time constant of 5 ms ±1. The step function response of the syllabic filter shall be exponential in nature. When the output of the overload algorithm is true, a charge curve shall be applicable. When the output of the overload algorithm is false, a discharge curve shall be applicable.

5.7 Reconstruction Integrator Time Constant. The reconstruction integrator shall have a time constant of 1 ms ±0.25.

5.8 Analog-to-Digital Conversion. An 800-Hz ±10 signal at a 0 dBm0 level applied to the input of the encoder shall give a duty cycle (C_d) of 0.30 at the algorithm output of the encoder shown in figure F-la.

5.9 Digital-to-Analog Conversion. The characteristics of a digital-to-analog conversion are described in the following subparagraphs.

5.9.1 Relation of Output to Input. With the applicable reference digital patterns of table F-1 applied to the digital input of the decoder as shown in figure F-3, the analog output signal shall be 800 Hz ±10 at the levels shown in table F-1, measured at the decoder output. These digital patterns, shown in hexadecimal form, shall be repeating sequences.

5.9.2 Conversion Speed. When the decoder input is switched from the 0-percent run-of-threes digital pattern to the 30-percent run-of-threes digital pattern, the decoder output shall reach 90 percent of its final value within 9 to 14 ms. When the decoder input is switched from the 30-percent run-of-threes digital pattern to the 0-percent run-of-threes digital pattern, the decoder output shall reach 10 percent of the 30-percent run-of-threes value within 6 to 9 ms. These values shall apply to both the 16 and 32-kbps data signaling rates.

5.10 CVSD Converter Performance. The characteristics specified in subparagraphs 5.10.1 through 5.10.7 apply to one CVSD conversion process obtained by connecting the output of an encoder to the input of a decoder (see figure F-3).

NOTE

Test signal frequencies which are submultiples of the data signaling rate shall be avoided by offsetting the nominal test frequency slightly; for example, an 800-Hz test frequency could be offset to 804 Hz. This test frequency offset will avoid nonlinear distortion which can cause measurement difficulties when tandeming CVSD with PCM.

TABLE F-1. DECODER REFERENCE DIGITAL PATTERNS FOR CVSD

Data Signaling Rate, kpbs	Digital Pattern	Run-of-threes, Percent	Output, dBm0
16	DB492	0	-24±1
32	DB54924AB6	0	-24±1
16	FB412	30	0±1
32	FDAA10255E	30	0±1

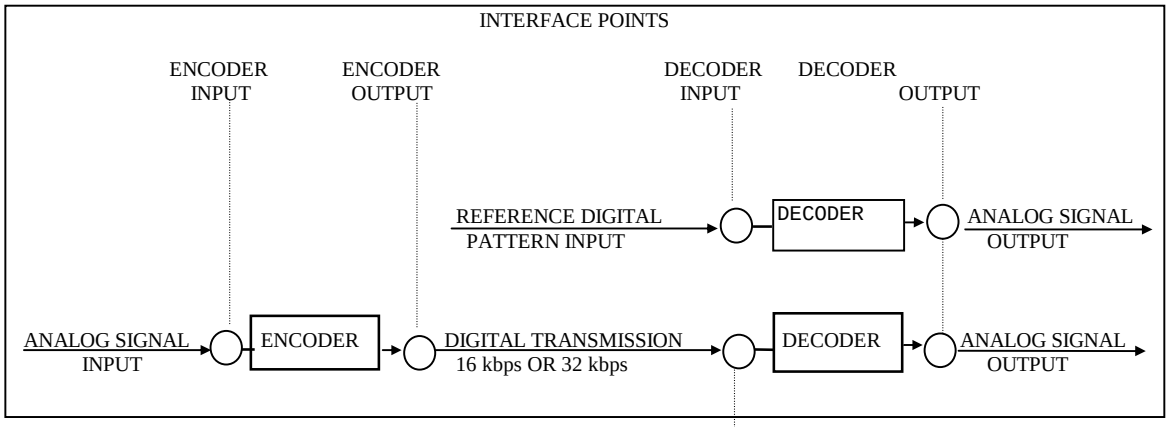

Figure F-3. Interface diagram for CVSD converter.

5.10.1 Companding Speed. When an 800-Hz ±10 sine wave signal at the encoder input is switched from -24 dBm0 to 0 dBm0, the decoder output signal shall reach 90 percent of its final value within 9 to 14 ms.

5.10.2 Insertion Loss. The insertion loss between the encoder input and the decoder output shall be 0 dB ± 2 dB with an 800 Hz ±10, 0 dBm0 input to the encoder.

5.10.3 Insertion Loss Versus Frequency Characteristics. The insertion loss between the encoder input and decoder output, relative to 800 Hz ±10 measured with an input level of -15 dBm0 applied to the converter input, shall not exceed the limits indicated in table F-2 and shown in figures F-4a and b.

TABLE F-2. INSERTION LOSS LIMITS FOR CVSD		
Rate, kpbs	**Frequency (f), Hz**	**Insertion Loss, dB (Referenced to 800 Hz)**
16	f < 300	≥ -1.5
	300 ≤ f ≥ 1000	-1.5 to 1.5
	1000 ≤ f ≥ 2600	-5 to 1.5
	2600 ≤ f ≥ 4200	≥ -5
	4200 ≤ f	≥ 25
32	f < 300	≥ -1
	300 ≤ f ≥ 1400	-1 to 1
	1400 ≤ f ≥ 2600	3 to 1
	2600 ≤ f ≥ 3400	3 to 2
	3400 ≤ f ≥ 4200	≥ -3
	4200 ≤ f	≥ 25

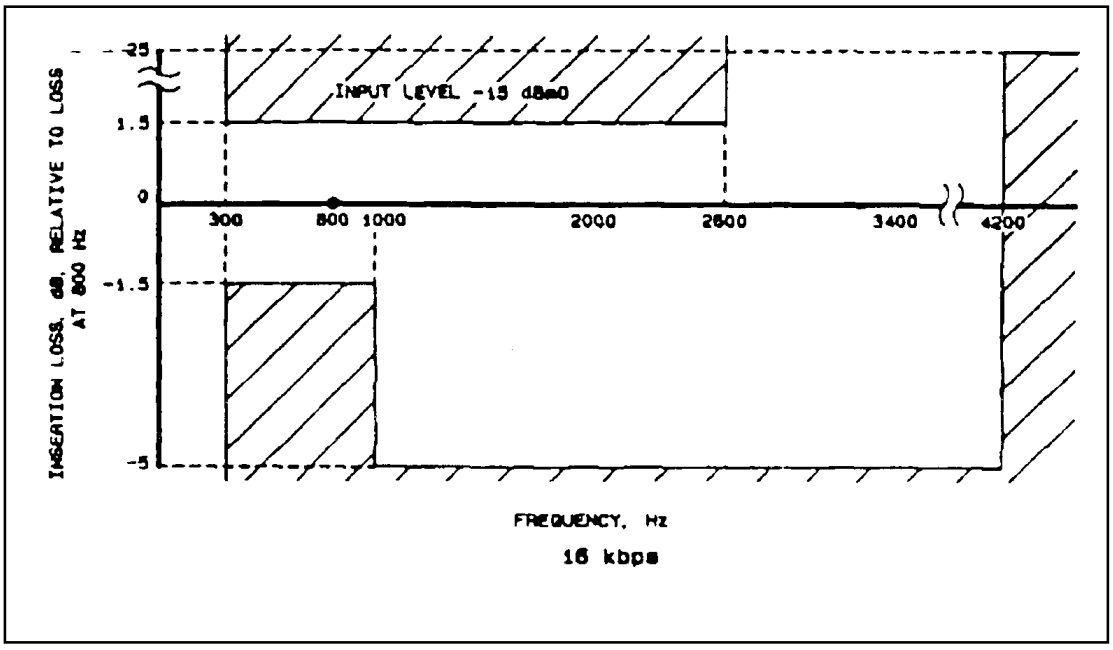

Figure F-4a. Insertion loss versus frequency for CVSD (16 kbps).

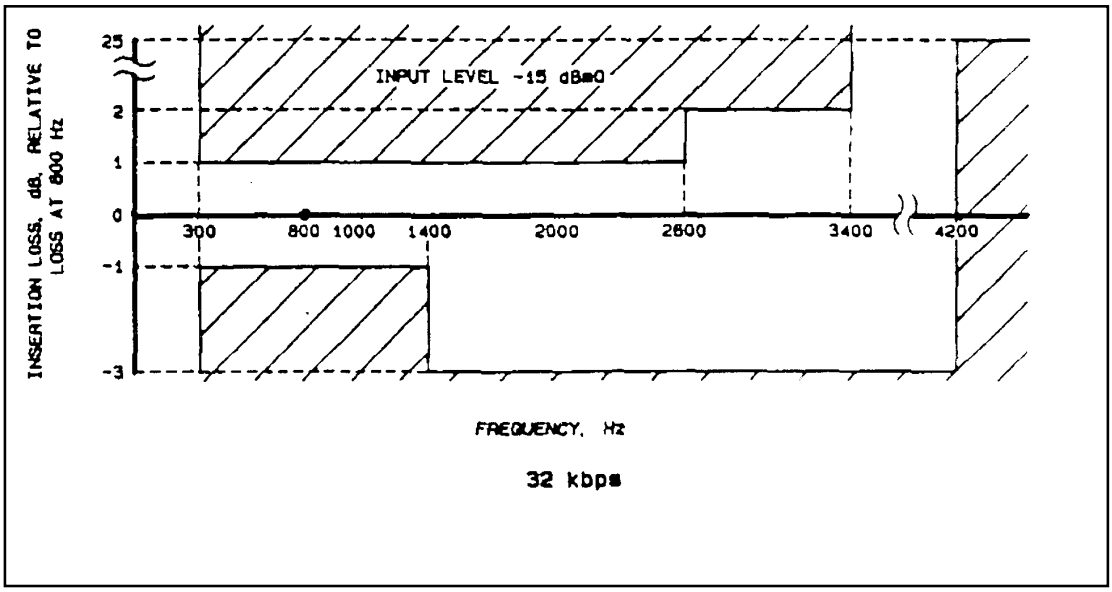

Figure F-4b. Insertion loss versus frequency for CVSD (32 kbps).

5.10.4 Variation of Gain With Input Level. The variation in output level, relative to the value at -15 dBm0 input, shall be within the limits of figure F-5a and b for an input frequency of 800 Hz ±10.

5.10.5 Idle Channel Noise. The idle channel noise shall not exceed the limits shown in table F-3 when measured at the CVSD decoder output.

5.10.6 Variation of Quantizing Noise With Input Level. The minimum signal to quantizing noise ratio over the input signal level range shall be above the limits of figure F-6a and b. The noise ratio shall be measured with flat weighting (unweighted) at the decoder output with a nominal 800-Hz ±10 sine wave test signal at the encoder input.

5.10.7 Variation of Quantizing Noise With Frequency. The minimum signal to quantizing noise ratio over the input frequency range shall be above the limits of figure F-7a and b. The noise ratio shall be measured with flat weighting (unweighted) at the decoder output with a sine wave test signal of -15 dBm0.

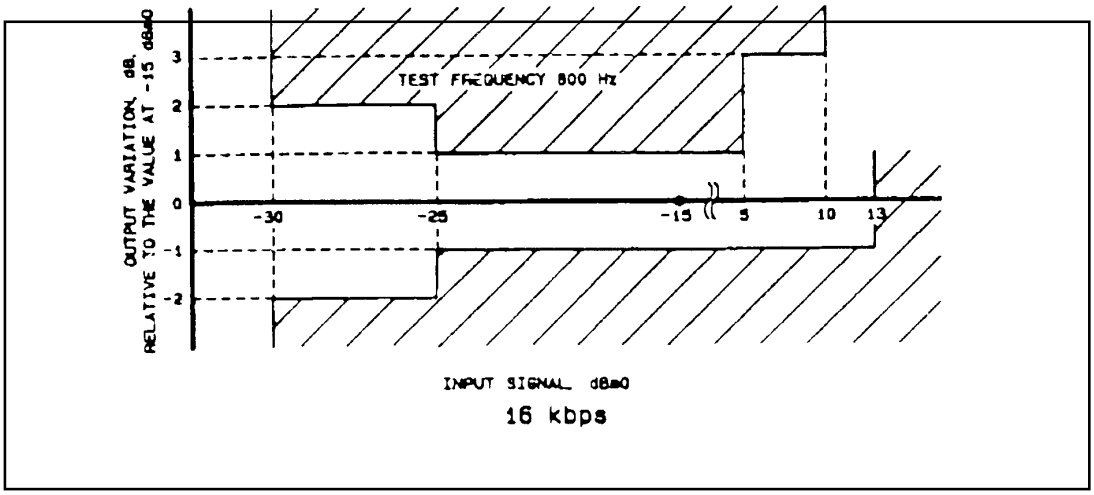

Figure F-5a. Variation of gain with input level for CVSD (16 kbps).

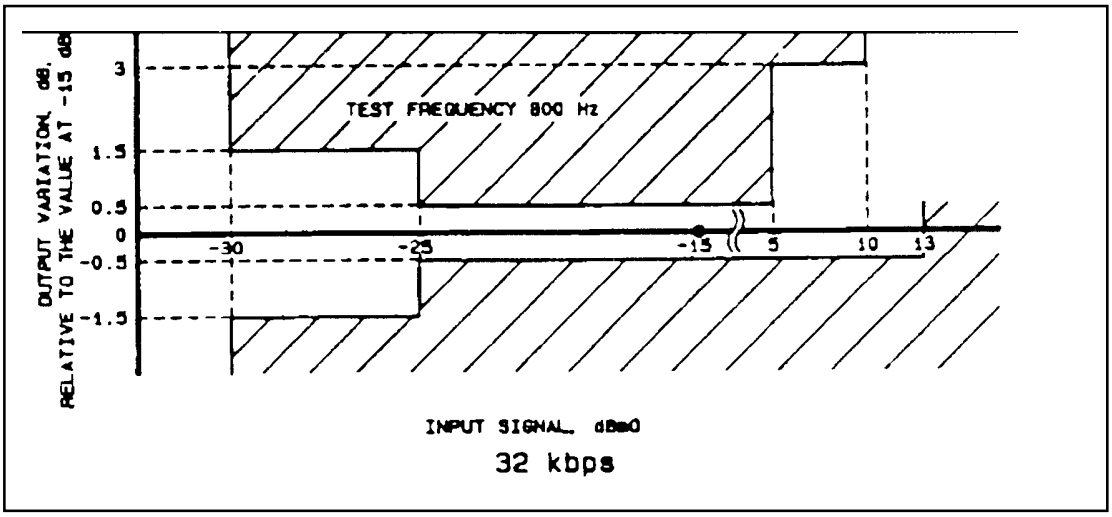

Figure F-5b. Variation of gain with input level for CVSD (32 kbps).

TABLE F-3. IDLE CHANNEL NOISE LIMITS FOR CVSD	
Data Signaling Rate, kbps	**Idle Channel Noise, dBm0**
16	-40
32	-50

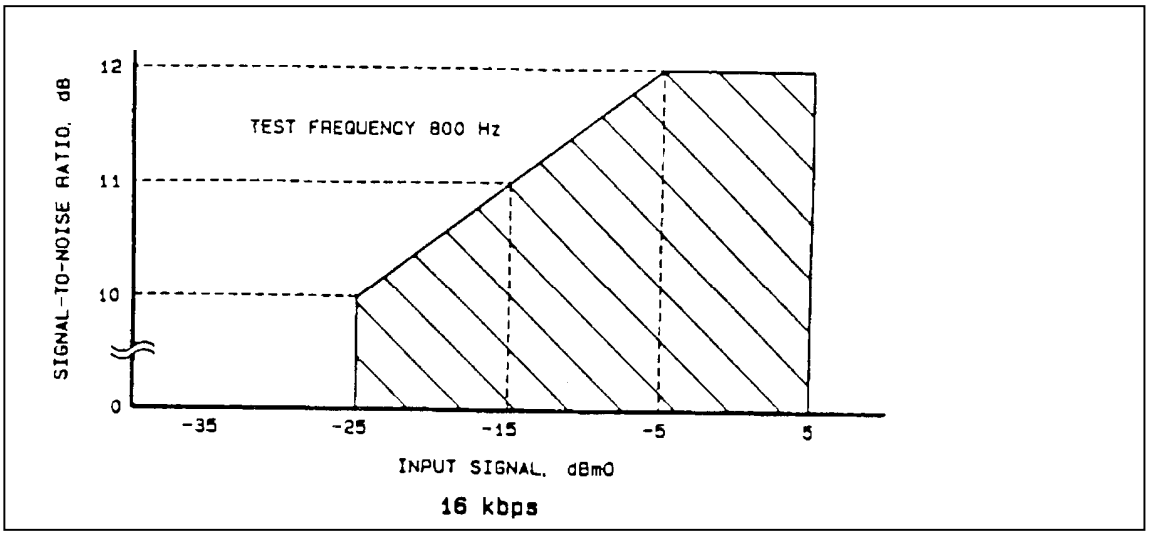

Figure F-6a. Signal to quantizing noise ratio versus input level for CVSD (16 kbps).

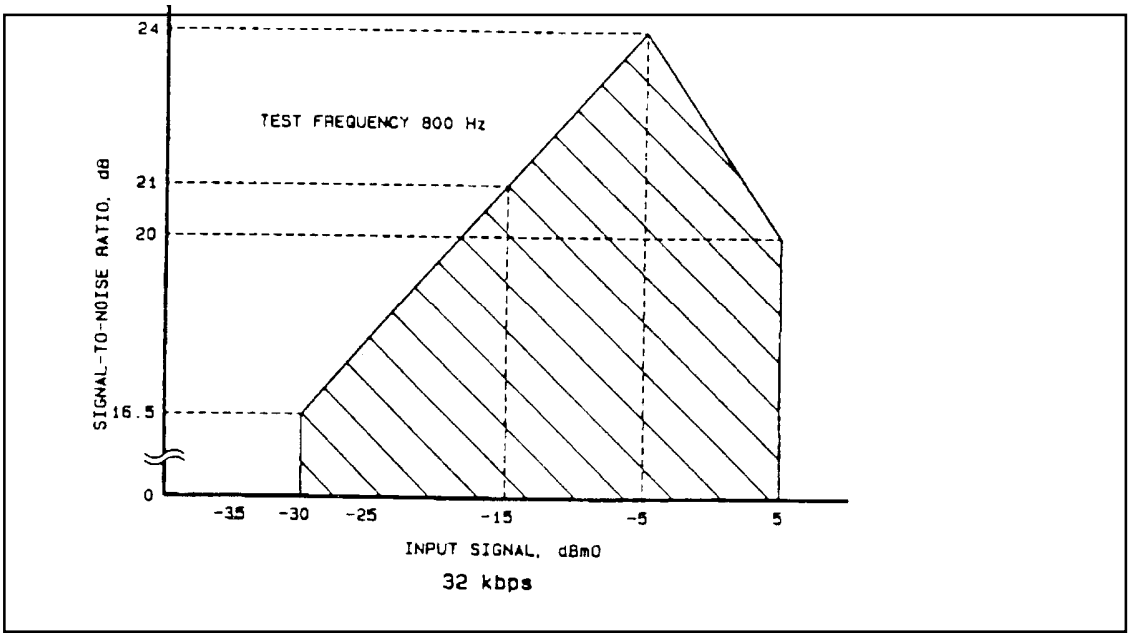

Figure F-6b. Signal to quantizing noise ratio versus input level for CVSD (32 kbps).

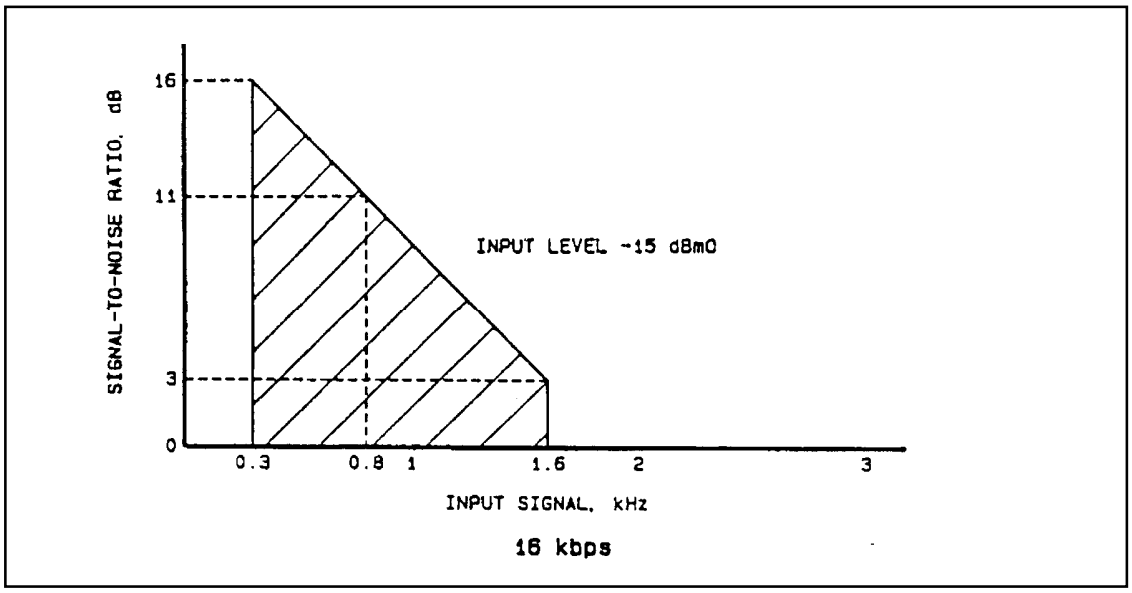

Figure F-7a. Signal to quantizing noise ratio versus frequency for CVSD (16 kbps).

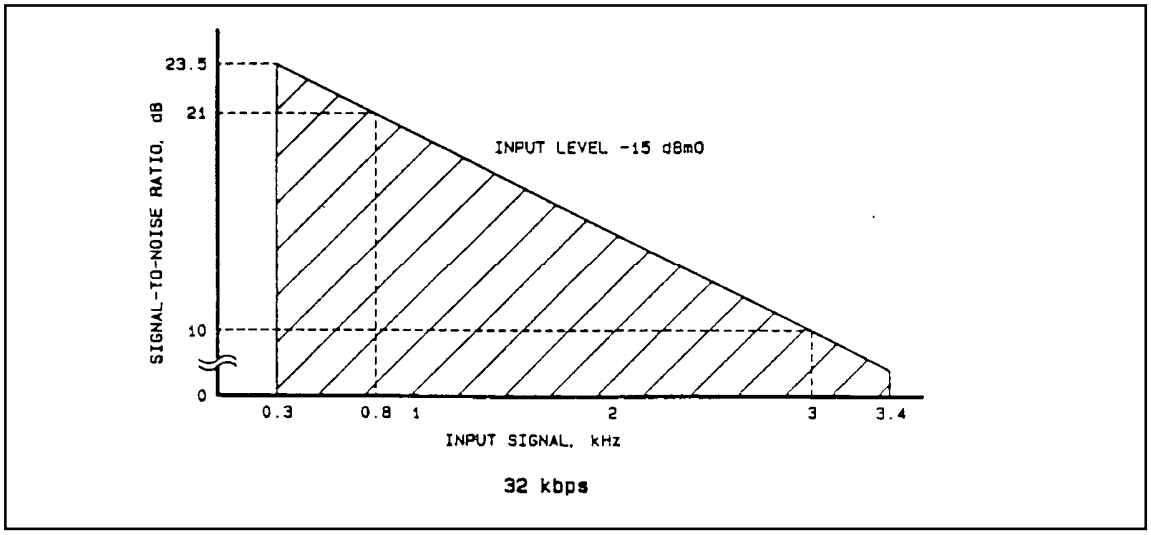

Figure F-7b. Signal to quantizing noise ratio versus frequency for CVSD (32 kbps).

APPENDIX G

ADARIO DATA BLOCK FIELD DEFINITIONS

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ADARIO DATA BLOCK FIELD DEFINITIONS

The details of the ADARIO data block format are provided in figure G-1 and in the ADARIO data format field summary. As shown in figure G-1, the eight session header words are the first eight words of the block. The channel packet for the highest priority (priority 1) channel is next, followed by the next lower priority channel packet (priority 2). Following the lowest priority channel, fill data consisting of all ones are inserted as required to complete the 2048-word data block.

Within the channel packet, the first five words are the channel header words including the partial word (PW). Following the channel header is the variable size channel data field. The channel data are organized in a last-in-first-out (LIFO) fashion. The first samples acquired in the block time interval appear in the last data word of the channel packet. The sample data are formatted into the 24-bit data word such that the first sample occupies the MSBs of the word. The next sample is formatted into the next available MSBs and so on until the word is full. As an example, data formatted into 8-bit samples is shown in figure G-2.

In cases where the 24-bit data word is not a multiple of the sample size, the sample boundaries do not align with the data words. In these cases, the samples at the word boundaries are divided into two words. The MSBs of the sample appear in LSBs of the first buffered word and the LSBs of the sample appear in the MSBs of the next buffered word. Since the channel data appears in a LIFO fashion in the ADARIO data block, the MSBs of the divided sample will occur in the data word following the word containing LSBs of the sample. Figure G-3 depicts ADARIO timings.

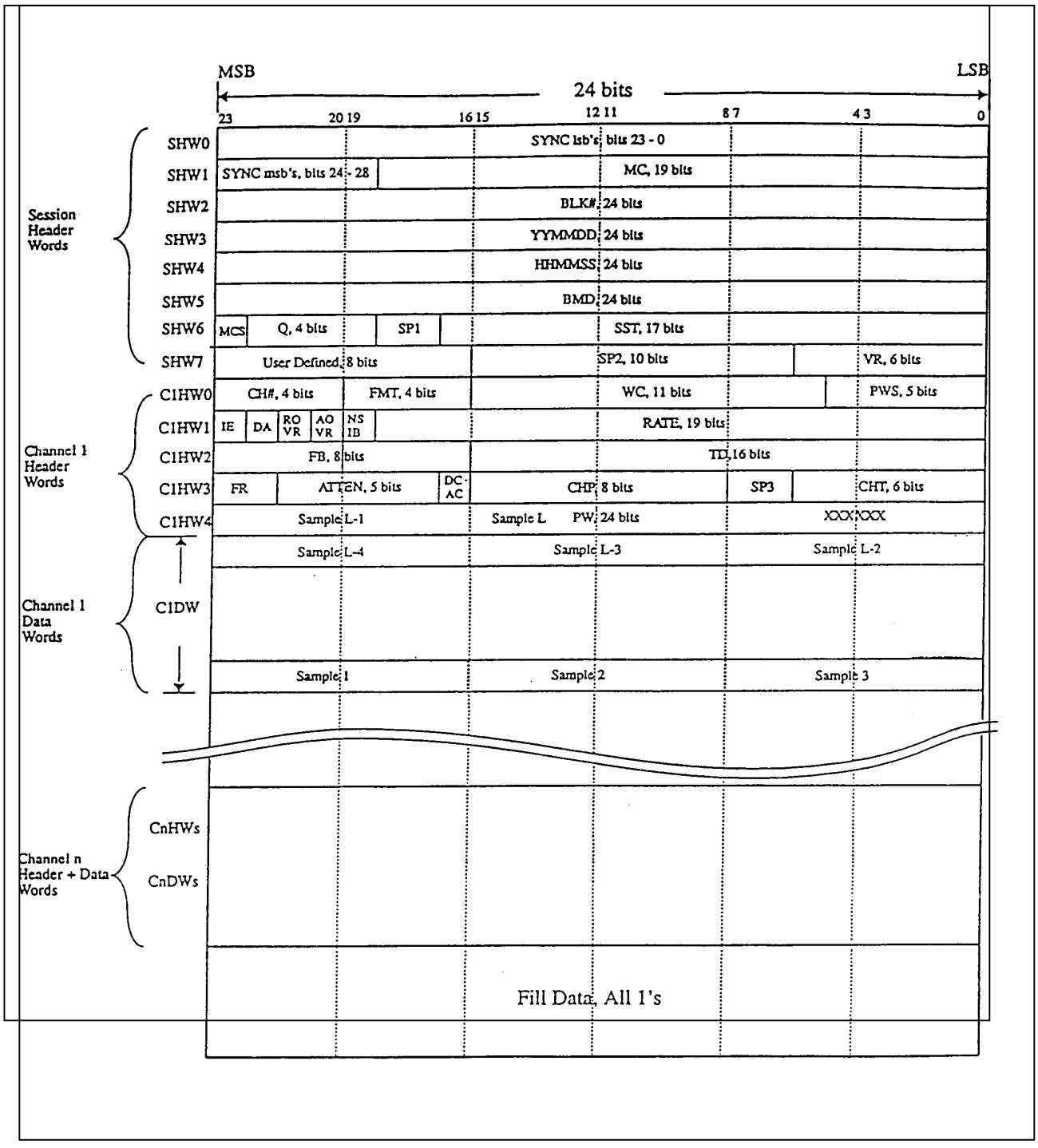


Figure G-1. ADARIO data format.

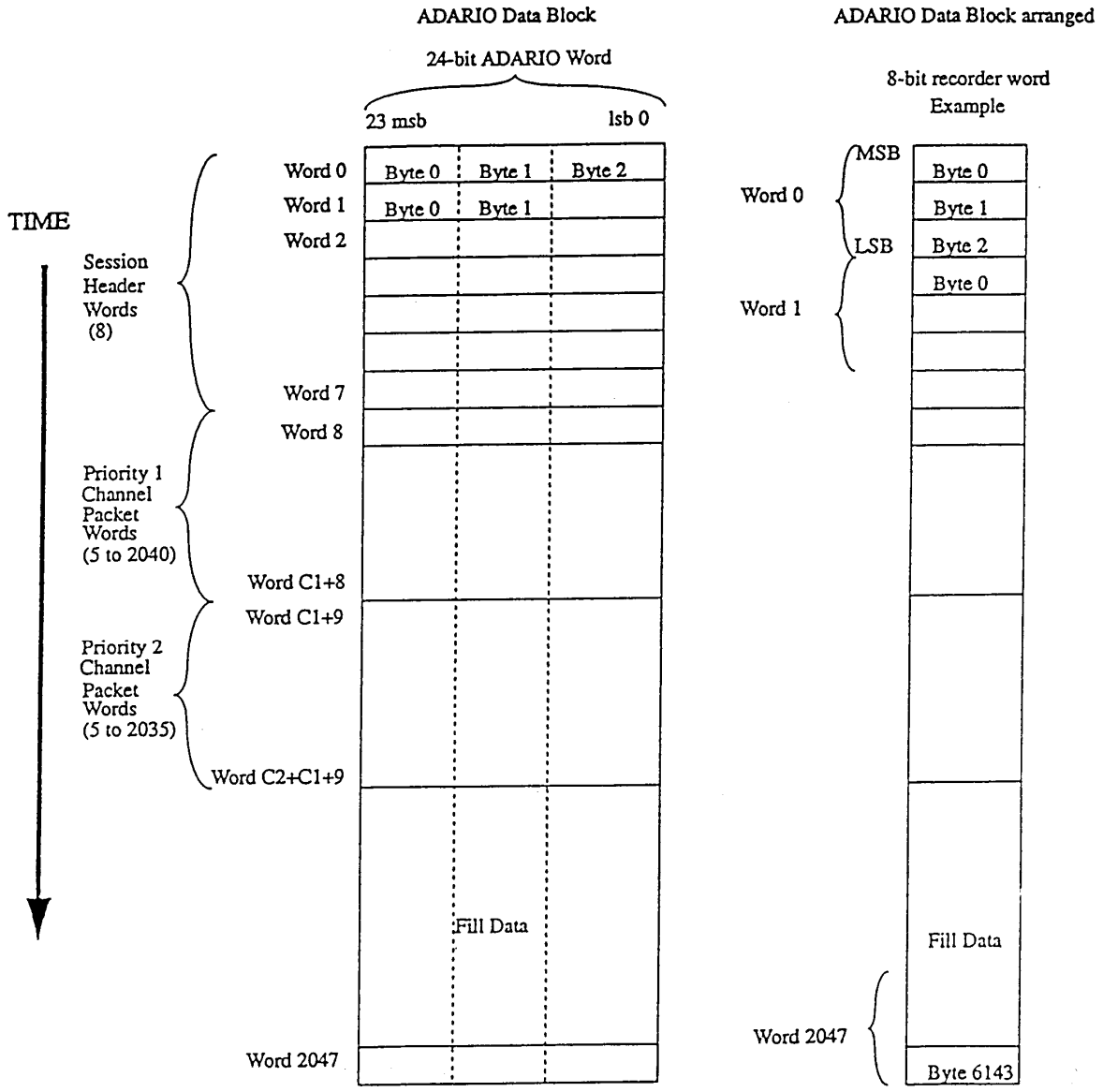


Figure G-2. ADARIO data blocks.

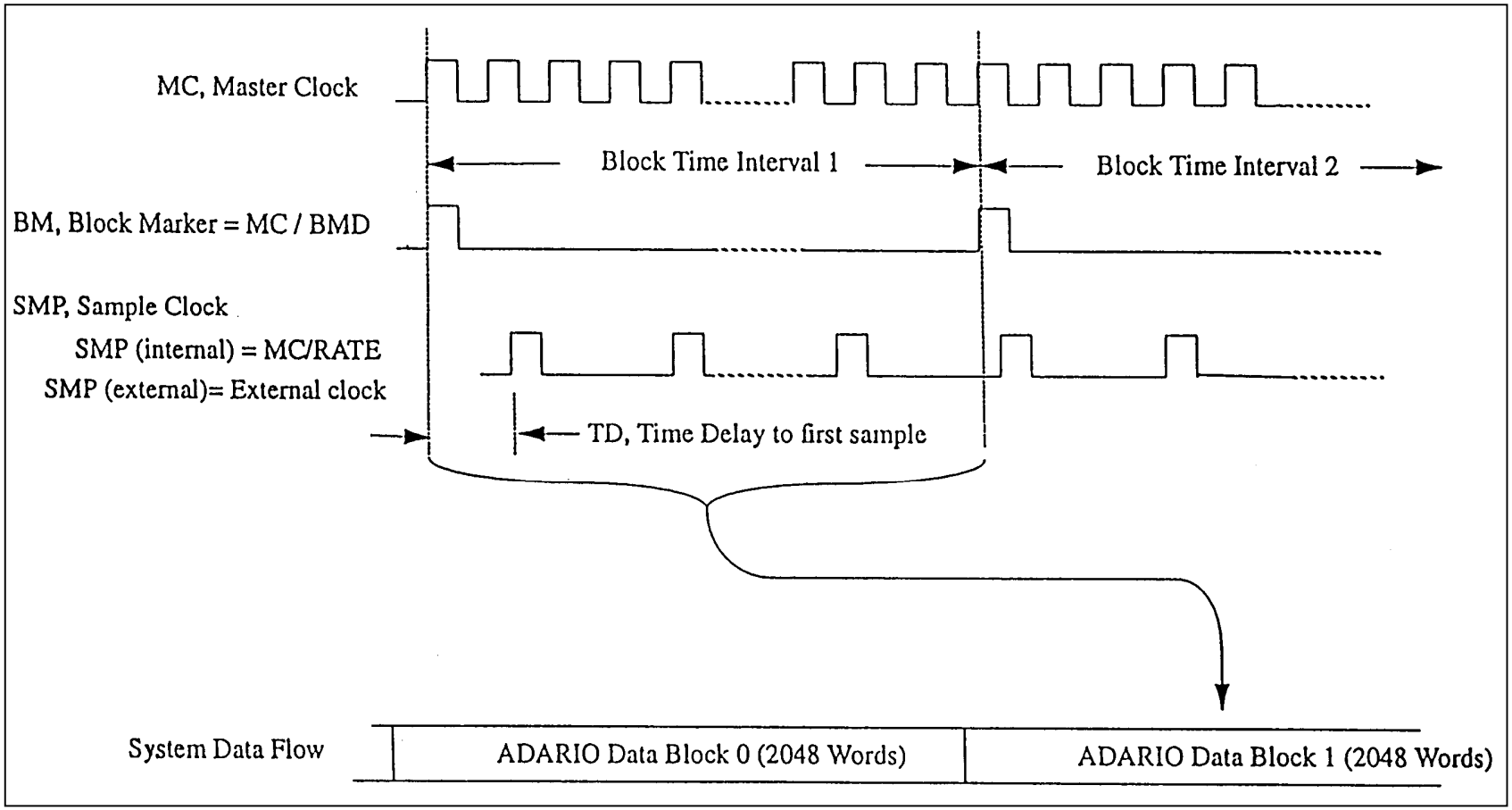


Figure G-3. ADARIO timing

ADARIO Data Format Field Definitions Summary

1. Block Length - (2048 words, 24-bit words, fixed length)

2. Session Header - (8 words, fixed format)

SHWO	(bits 23 to 0)	SYNC Field, bits 0-23 of the 29-bit block sync. The LSBs of the block sync are 36E19C and are contained here.
SHW1	(bits 23 to 19)	SYNC Field, bits 24-28 of the 29-bit block sync. The MSBs of the block sync are 01001 and are contained here. The 29-bit block sync is fixed for all ADARIO configurations and chosen for minimal data cross correlation.
	(bits 18 to 0)	MC, Master Clock, a 19-bit binary value in units of 250 Hz. MC is the clock frequency used to derive session and per channel parameters.
SHW2	(bits 23 to 0)	BLK#, ADARIO Data Block Number, a 24-bit binary value. BLK# is to zero at the start of each session and counts up consecutively. Rollover is allowed.
SHW3	(bits 23 to 0)	YYMMDD, Time Code Field, a BCD representation of the year (YY), month (MM), and day (DD). YYMMDD Time Code Field is updated during the record process once per second.
SHW4	(bits 23 to 0)	HHMMSS, Time Code Field, a BCD representation of the hour (HH), minute (MM), and second (SS). The HHMMSS Time Code Field is updated during the record process once per second.
SHW5	(bits 23 to 0)	BMD, Block Marker Divisor, a 24-bit binary value. BMD is established so that the block marker frequency, BM, may be derived from MC by BM = MC/BMD

SHW6	(bit 23)	MCS, Master Clock Source, a 1-bit flag. 1 = MC was generated internally. 0 = MC was provided from an external source.
	(bits 22 to 19)	Q, Number of active channels minus one, a 4-bit binary value. For example, 0 indicates that one channel is active.
	(bits 17 to 18)	SP1, Spare field 1, a 2-bit field. It is set to zero.
	(bits 16 to 0)	SST, Session Start Time, a 17-bit binary value in units of seconds. The integer number of seconds represents the session start time of day in seconds, where midnight starts with zero.
SHW7	(bits 23 to 16)	User Defined, an 8-bit field. May be input by the user at any time during a recording session. The interpretation of this bit field is left to the user.
	(bits 15 to 6)	SP2, Spare field 2, a 10-bit field. It is set to zero.
	(bits 5 to 0)	VR, Version number, a 6-bit binary value. Each update of the ADARIO format will be identified by a unique version number.

3. Channel ‘n’ Header

All channel headers contain five 24-bit ADARIO words with the following fixed format. The first logical channel, n=1, has the highest priority and its channel packet starts in the ninth word of the data block. Each active channel is represented by a channel packet that is present in the data block. The logical channel number, n, represents the relative priority of the channel and the order in which it appears in the data block.

CnHW0	(bits 23 to 20)	CH#, Physical Channel Number, a 4-bit binary value. 0 to 15 represents the physical location of the channel electronics in the ADARIO hardware. The user sees those locations labeled from 1 to 16.
	(bits 19 to 16)	FMT, Format code for the channel data word, a 4-bit binary value. The format code is used to define the size of the user data word by means of the following table:

15=24 bits	7=8 bits
14=22 bits	6=7 bits
13=20 bits	5=6 bits
12=18 bits	4=5 bits
11=16 bits	3=4 bits
10=14 bits	2=3 bits
9=12 bits	1=2 bits
8=10 bits	0=1 bit

	(bits 15 to 5)	WC, Word Count, an 11-bit binary value. WC is the number of full channel data words that should be in the nth channel packet. WC may range from 0 to 2040. A WC greater than the number of actual words in channel packet indicates a data rate overflow, which would occur when a low-priority channel is not provided sufficient space in the fixed length data block as a result of an uncontrolled data rate in a higher priority channel.
	(bits 4 to 0)	PWS, Partial Word Status, a 5-bit binary value. PWS is related to the number of samples in the partial word and may range from 0 to 23. PWS shall be computed as follows: If the number of full samples in the partial word equals zero, then PWS = 0. If the number of full samples in the partial word does not equal zero, then PWS = Round Up [Unused bits In PW/Channel Sample Size].

CnHW1	(bit 23)	IE, Channel Clock Source, a 1-bit flag. 1 = The channel clock was generated internally. 0 = The channel clock was provided from an external source.
	(bit 22)	DA, Data type, a 1-bit flag. 1 = The channel is operated as a digital channel. 0 = The channel is operated as an analog channel.
	(bit 21)	ROVR, Rate overrun in previous block, a 1-bit flag. 1 = The nth channel packet in the previous data block experienced an overrun. 0 = The nth channel packet in the previous data block did not experience an overrun.
	(bit 20)	AOVR, Analog A/D Overrange in current block a 1-bit flag. 1 = The nth channel in the current data block experienced an analog-to-digital conversion overrange condition. 0 = The nth channel in the current data block did not experience an analog-to-digital conversion overrange condition.
	(bit 19)	NSIB, No samples in current block, a 1-bit flag. 1 = TRUE, there are no samples for the nth channel in the current block. 0 = False, there are samples for the nth channel in the current block.

The definitions that are marked with an asterisk apply to analog channels and to particular hardware implementations of ADARIO. For the purposes of this standard these fields are not used.

	(bits 18 to 0)	RATE, Channel sample rate indicator, 19-bit binary value. The interpretation of the rate value depends on the condition of IE, the channel clock source flag.

			If IE = 1, then the value of rate is carried by the 16 LSBs of the rate field. Using rate, the frequency of the internal channel clock can be found by internal sample clock = (MC/RATE) -1. IF IE = 0, then rate is a 19-bit binary value in units of 250 Hz which equals the frequency of the external channel clock as provided by the user at the time of the setup.
*	CnWD2	(bits 23 to 16)	FB, Filter Bandwidth, an 8-bit binary value. The formula for the bandwidth, BW, of the anti-aliasing filter used in an analog channel incorporates FB as BW = (FB/2) X 10^{3+FR}
		(bits 15 to 0)	TD, Time Delay to first sample, a 16-bit binary value. TD is a measure of the time delay from the block marker, BM, to the first sample arriving at the nth channel during the current data block interval. TD is expressed as the number of master clock, MC, periods minus one.
*	CnWD3	(bits 23 to 22)	FR, Filter Range, a 2-bit binary value. The formula for the bandwidth, BW, of the anti-aliasing filter used in an analog channel corporates FR as BW = (FB/2) X 10^{3+FR}
		(bits 21 to 17)	ATTEN, Attenuation, a 5-bit binary value. ATTEN represents the setting of the input attenuator (or gain) on the nth channel at the time that the record was formed 0=-15dB and 31 = +16dB with intermediate settings expressed in one dB steps.
		(bit 16)	DCAC, Analog signal coupling, a 1-bit flag. 1 = The channel is operated with dc coupling at the input. 0 = The channel is operated with ac coupling at the input.
		(bits 15 to 8)	CHP, Channel Parameter field, an 8-bit field. The interpretation of the CHP field depends upon the card type with which it is associated, as defined by the CHT field. Each card type established by the CHT field, as part of its definition, shall specify the form and interpretation of the CHP field. To date,

four input card types have been established. The following CHP fields are defined as

* For CHT=0

(bits 15 to 8) remain undefined for the present analog single channel implementation except that the present hardware implementation expects an all zero field. Would be subject to future definition as long as all the zero fill is set aside.

* For CHT=1

(bits 15 to 8) remain unused for the present digital single channel implementations except that the present hardware implementation expects an all zero field. Would be subject to future definition as long as the all zero fill is set aside.

* For CHT=2

(bits 15 to 8) remain unused for the present dual-purpose channel implementations except that the present hardware implementation expects an all zero field. Would be subject to future definition as long as the all zero fill is set aside.

For CHT=3

(bits 15 to 12) establish the number of subchannels that are multiplexed into the multichannel data carried by the nth channel.

(bits 11 to 8) identify the subchannel number of the first sample contained in the nth channel packet of the data block.

(bits 7 to 6) SP3, Spare field 3, a 2-bit field. It is set to zero.

(bits 5 to 0) CHT, Channel Type, a 6-bit field. Defines the type of channel through which input data was acquired. Additional channel types to be defined by future users and developers.

* CHT=0 Single channel analog input
* CHT=1 Single channel digital input
- CHT=2 Single channel, dual-purpose, analog or digital input

		* CHT=3 Multichannel analog input capable of multiplexing up to 16 analog inputs * CHT=4 Single channel digital input, dual channel analog input (stereo) "L" Channel on bits 15 to 8 of the sample word, "R" channel on bits 7 to 0 of the sample word * CHT=5 Single channel, triple-purpose, analog, digital, submux, formatted input
CnWD4	(bits 23 to 0)	PW, Partial Word, A 24-bit field. PW contains the last samples of the data block. The most significant bits of word contain the first sample, followed by the next sample in the next most significant bits. The number of samples in the PW is defined in the PWS field. The unused bits are not intentionally set and so contain random data.
Fill	(bits 23 to 0)	Fill, Fill Words consisting of all ones binary, used for fixed rate aggregate. Fill words may be omitted when variable rate aggregate can be accommodated resulting in variable length blocks of up to 2048, 24-bit words.

SUBMUX DATA FORMAT FIELD DEFINITIONS

The details of the submux data format are shown in figures G-4a and b and defined in the Submux Data Format Field Definitions Summary. Figure G-5 shows a typical primary channel aggregate data content for fixed and variable rate channel. Submux data format is based on the sequential collection of the individual channel data blocks. Each channel data block is the sequential collection of presented input samples in a fixed period of time. This sequential collection results in a variable length, fixed rate, and channel data blocks. To accommodate fixed rate channels, fill is also defined. The aggregate data stream is composed of a block sync timing channel, followed by sequential channel data blocks, if enabled, followed by fill, if required, at fixed block rate.

The channel data blocks are the sequential collection of input samples bit packed into sequential 16-bit words over the block period of time. The data block is preceded by a three-word header that identifies the source (channel ID) of data, channel type of processing, packing format in the data block, bit count length of the valid data, and the time delay between the first sample and the block period. If data were internally sampled, the sample period is defined with the first sample being coincident with the start of block period. Channel type is used to define specific types of channels that provide timing, annotation, and synchronization functions that may be required by the specific primary channel or may be redundant and not required. Specific implementation of the required channels may provide only the required channels with specific implementation constraints that limit the aggregate rate or the range of any specific field.

The submux format is based on a 16-MHz clock defining all timing. The derived clock is the 16-MHz clock divided in binary steps as defined by 2^{BRC} that defines all timing and internal sampling. Block period is 20 160 derived clock periods which limits the submux aggregate to 256 Mbps, limits the maximum block rate to 793.65 blocks per second, and in conjunction with a 16-bit bit count field, limits the subchannel maximum data rate to 52 Mbps.

SUBMUX DATA FORMAT FIELD DEFINITIONS SUMMARY

1. Frame length — Variable or fixed with fill. Minimum is 3-word block sync plus one channel block, maximum is 20 160x16-bit words.

2. Block length — Variable from 3x16-bit words to 4099x16-bit words per channel data block. Specified by CHT>0 and integer of (Bit_Count+15/16). May be limited by implementation.

3. Block Sync — Defined by Channel ID = 31, 3-word block, 2-word sync. Defines a period of 20 160 derived clocks.

4. General Form — All Channel data blocks contain this information in the 3-word header.

   HW1 (bits 15 to 11) — CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel of any type. CHN ID = 31 reserved for Block Sync.

   (bits 10 to 8) — CHT, Channel Type, from 0 to 7 defines type of processing performed on the data and the format of header word fields.

CHT = 0	Timing channel, block sync or time tag, 3-word only
CHT = 1	Annotation text or block count, variable length
CHT = 2	Digital serial external or internal clock, variable
CHT = 3	Digital parallel external clock, variable
CHT = 4	Analog wide band, variable
CHT = 5	Analog stereo, variable
CHT = 6	TBD (to be defined by future implementation)
CHT = 7	TBD

Variable length		General form with variable data block length
HW1	(bits 15 to 11)	CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel of any type.
	(bits 10 to 8)	CHT, Channel Type, from 1 to 7 defines type of processing performed on the data and the format of header word fields.
	(bits 7 to 4)	FMT, Format, defines the number of bits minus one in each sample. Data block sample size (bits) = (FMT+1). Range 0 to 15, binary format.
	(bits 3 to 0)	ST1 to ST4, status bits, define dynamic conditions within this block period such as over range.
HW2	(bits 15 to 0)	Bit_Count defines the number of valid data bits in the data block starting with the most significant bit of the first data word DW1. Variable word length of the data block is the Integer of ((Bit_Count + 15)/16). Range 0 to 65535, binary format.
HW3	(bit 15)	I/E, Internal / External clock
	(bits 15 to 0)	Depends on CHT field, defines block count, time delay, or sample period.

5. Block Sync — Defines the start of channel data blocks and start of block period that lasts for 20 160 derived clocks.

HW1	(bits 15 to 0)	SYNC 1 = F8C7 hex, defines the first sync word.
HW2	(bits 15 to 0)	SYNC 2 = BF1E hex, defines the second sync word.
HW3	(bits 15 to 13)	BRC, Block Rate Clock, defines the binary divisor for the 16 MHz system clock. Derived CLK = 16 MHz / 2^{BRC} MHz. Block rate = Derived CLK / 20160 Hz. Period = 1 / Derived CLK.
	(bit 12)	FILL, indicates if the primary channel requires fill for constant rate.
	(bits 11 to 4)	TBD

	(bit 3)	AOE, Aggregate Overrun Error if set indicates that the aggregate of the enabled channels exceeds the submux aggregate (data truncated to 20 160 words between sync).
	(bit 2)	PCRE, Primary Channel Rate Error if set indicates that primary channel is unable to maintain the aggregate rate of the submux. Excess blocks are truncated.
	(bits 1 to 0)	ST3, ST4, Status reserved.

6. Time Tag — Defines the time tag channel for time stamping the frame.

HW1	(bits 15 to 11)	CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.
	(bits 10 to 8)	CHT = 0, Channel Type = 0, Time Tag IRIG Time code processing and 3-word format.
HW	(bits 7 to 0)	DAYS, Most significant 8 bits of Time Code Days field. BCD format.
	(bits 15 to 14)	DAYS, Least significant 2 bits of Time Code Days field. BCD format.
	(bits 13 to 8)	HOURS, Time Code Hours 6 bit field. BCD format.
HW	(bits 7 to 0)	MINUTES, Time Code Minutes 7 bit field. BCD format.
	(bits 15 to 8)	SECONDS, Time Code Seconds 7 bit field. BCD format.
	(bits 7 to 0)	FRACTIONAL SECONDS, Time Code Fractional Seconds 8 bit field. BCD format.

7. Annotation Text — Defines block count and annotation text that pertains to the subchannels at this time.

HW1	(bits 15 to 11)	CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.
	(bits 10 to 8)	CHT = 1, Channel Type = 1, Block Count and Annotation Text if any.
	(bits 7 to 4)	FMT = 7, Format = 7 , defines 8 bit ASCII character in text.
	(bit 3)	NC, No Characters (Bit_Count = 0) Block count only.
	(bits 2 to 0)	OVR, PE, OE, Overrun Parity and async framing error.
HW	(bits 15 to 0)	Bit_Count defines the number of valid data bits in the data block starting with the MSB of the first data word DW1. Variable word length of the data block is the Integer of ((Bit_Count + 15)/16). Range 0 to 65 535, binary format.
HW	(bits 15 to 0)	Block_Count sequential block numbering with rollover at maximum. Range 0 to 65 535, binary format.
DW1	(bits 15 to 8)	1st CHARACTER, first text character.
DW	(bits 8 or 0)	Last CHARACTER, LSB is defined by the Bit Count.

8. Digital Serial External CLK — Defines digital serial data such as PCM externally clocked.

HW1	(bits 15 to 11)	CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.
	(bits 10 to 8)	CHT = 2, Channel Type = 2, digital serial or data and clock over sampled data.
	(bits 7 to 4)	FMT = 0 Format = 0, defines 1-bit data samples.
	(bit 3)	NSIB, No Samples In Block (Bit_Count=0) header only.
	(bit 2)	OVR, Overrun indicates that input is clocking at faster than specified rate. Data is truncated at specified bit rate (Bit Count per Block).
HW	(bits 15 to 0)	Bit_Count, defines the number of valid data bits in the data block starting with the most significant bit of the first data word DW1. Variable word length of the data block is the Integer of ((Bit_Count + 15)/16). Range 0 to 65 535, binary format. Limited by set maximum rate.
HW	(bit 15)	I/E = 0, Internal / External clock flag indicates that external clocking was used with relative phasing to block as specified in next field.
	(bits 14 to 0)	Time Delay provides the measure of time between start of block period and the first external clock in derived clock periods. Range 0 to 20 160, binary format.
DW1	(bit 15)	DS_1, first data sample at the first clock time in the block.
Dw_n	(bit L)	DS_L, last data sample in this block period.

9. Digital Serial Internal CLK — Defines digital serial data low rate (> 2 samples per block period) internally oversampled.

HW1	(bits 15 to 11)	CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.
	(bits 10 to 8)	CHT = 2, Channel Type = 2, Digital serial or data and clock over sampled data.
	(bits 7 to 4)	FMT = 0 Format = 0, defines 1-bits data samples.
	(bits 3 to 0)	0, reserved.
HW2	(bits 15 to 0)	Bit_Count defines the number of valid data bits in the data block starting with the most significant bit of the first data word DW1. Variable word length of the data block is the Integer of ((Bit_Count + 15)/16). Range 0 to 65 535, binary format. Limited by set maximum rate.
HW3	(bit 15)	I/E = 1, Internal Sampling flag indicates that internal sampling was used as specified in next field.
	(bits 14 to 9)	TBD

	(bits 8 to 0)	SAMPLE PERIOD, defines the period of the over-sampling clock that samples data and clock, in derived clock periods. Range 0 to 4 mega samples per second, binary format.
DW1	(bit 15)	DS_1, first data sample at block time.
	(bit 7)	CS_1, first clock sample at block time.
DWn	(bit 8)	DS_L, last data sample in this block period.
	(bit 0)	CS_L, last clock sample in this block period.

10. Digital Parallel External CLK — Defines digital data including serial externally clocked.

HW1	(bits 15 to 11)	CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.
	(bits 10 to 8)	CHT = 3, Channel Type = 3, Digital parallel or serial data.
	(bits 7 to 4)	FMT, Format, defines the number of bits minus one in each sample. Data block sample size (bits) = (FMT+1). Range 0 to 15, binary format.
	(bit 3)	NSIB, No Samples In Block (Bit_Count = 0) Header only.
	(bit 2)	OVR, Overrun indicates that input is clocking at faster than specified rate. Data is truncated at specified bit rate (Bit Count per Block).
HW2	(bits 15 to 0)	Bit_Count defines the number of valid data bits in the data block starting with the most significant bit of the first data word DW1. Variable word length of the data block is the Integer of ((Bit_Count + 15)/16). Range 0 to 65 535, binary format. Limited by set maximum rate.
HW3	(bit 15)	I/E = 0, Internal / External clock flag indicates that external clocking was used with relative phasing to block as specified in next field.
	(bits 14 to 0)	Time delay provides the measure of time between start of block period and the first external clock in derived clock periods. Range 0 to 20 160, binary format.
DW1	(bit 15)	DS_1, MSB of the first data sample at the first clock time in the block.
DW_n	(bit L)	DS_L, LSB of the last data sample in this block period.

11. Analog Wide Band — Defines analog wide band data using a sampling A/D and internal block synchronous clock.

HW1	(bits 15 to 11)	CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.

	(bits 10 to 8)	CHT = 4, Channel Type = 4, analog wide band sampled data.
	(bits 7 to 4)	FMT, Format, defines the number of bits minus one in each sample. Data block Sample Size (bits) = (FMT+1). Range 0 to 15, binary format. Limited by the A/D resolution.
	(bit 3)	AOR, Analog over range (A/D 4-msb = F).
	(bits 2 to 0)	ST2 to ST4, reserved status
HW2	(bits 15 to 0)	Bit_Count defines the number of valid data bits in the data block starting with the MSB of the first data word DW1. Variable word length of the data block is the Integer of ((Bit_Count + 15)/16). Range 0 to 65 535, binary format. Limited by set maximum rate.
HW3	(bit 15)	I/E = 1, Internal Sampling flag indicates that internal sampling was used as specified in next field.
	(bits 14 to 12)	TBD
	(bits 11 to 0)	Sample Period defines the period of the over-sampling clock that samples data and clock, in derived clock periods. Range 0 to 4m samples per second, binary format.
DW1	(bit 15)	DS_1, MSB of the first data sample at the first clock time in the block.
DW_n	(bit L)	DS_L, LSB of the last data sample in this block period.

12. Analog Stereo "L" & "R" — Defines analog stereo data using a sigma-delta A/D and internal block synchronous clock with tracking Finite Impulse Response (FIR) filter.

HW1	(bits 15 to 11)	CHN ID, Channel ID number, from 0 to 30 binary number represents normal channel.
	(bits 10 to 8)	CHT = 5, Channel Type = 5, Analog stereo voice band data.
	(bits 7 to 4)	FMT, Format defines the number of bits minus one in each sample. Data block sample size (bits) = (FMT+1). Range 0 to 15, binary format. Limited by the A/D resolution.
	(bit 3)	LAOR, left subchannel over range.
	(bit 2)	RAOR, right subchannel over range.
	(bits 1 to 0)	ST2 to ST4, reserved status.
HW2	(bits 15 to 0)	Bit_Count defines the number of valid data bits in the data block starting with the MSB of the first data word DW1. Variable word length of the data block is the Integer of ((Bit_Count + 15)/16). Range 0 to 65 535, binary format. Limited by set maximum rate.

HW3	(bit 15)	I/E = 1, Internal Sampling flag indicates that internal sampling was used as specified in next field.
	(bit 14)	ENL, Enable Left subchannel.
	(bit 13)	ENR, Enable Right subchannel.
	(bit 12)	TBD
	(bits 11 to 0)	Sample period defines the period of the over-sampling clock that samples data and clock, in derived clock periods. Range 3.76 to 40K samples per second, binary format.
DW1	(bit 15)	DS_1, MSB of the first data sample left subchannel if enabled.
	(bit 15-FMT-1)	DS_1, MSB of the first data sample right subchannel if enabled, else second sample.
DWn	(bit L)	DS_L, LSB of the last data sample in this block period.

13. Fill — Defines fill word that can be inserted at the end of all channel data blocks if required by the constant rate primary channel.

Fwx (bits 15 to 0)	FILL, defined as FFFF hex word.

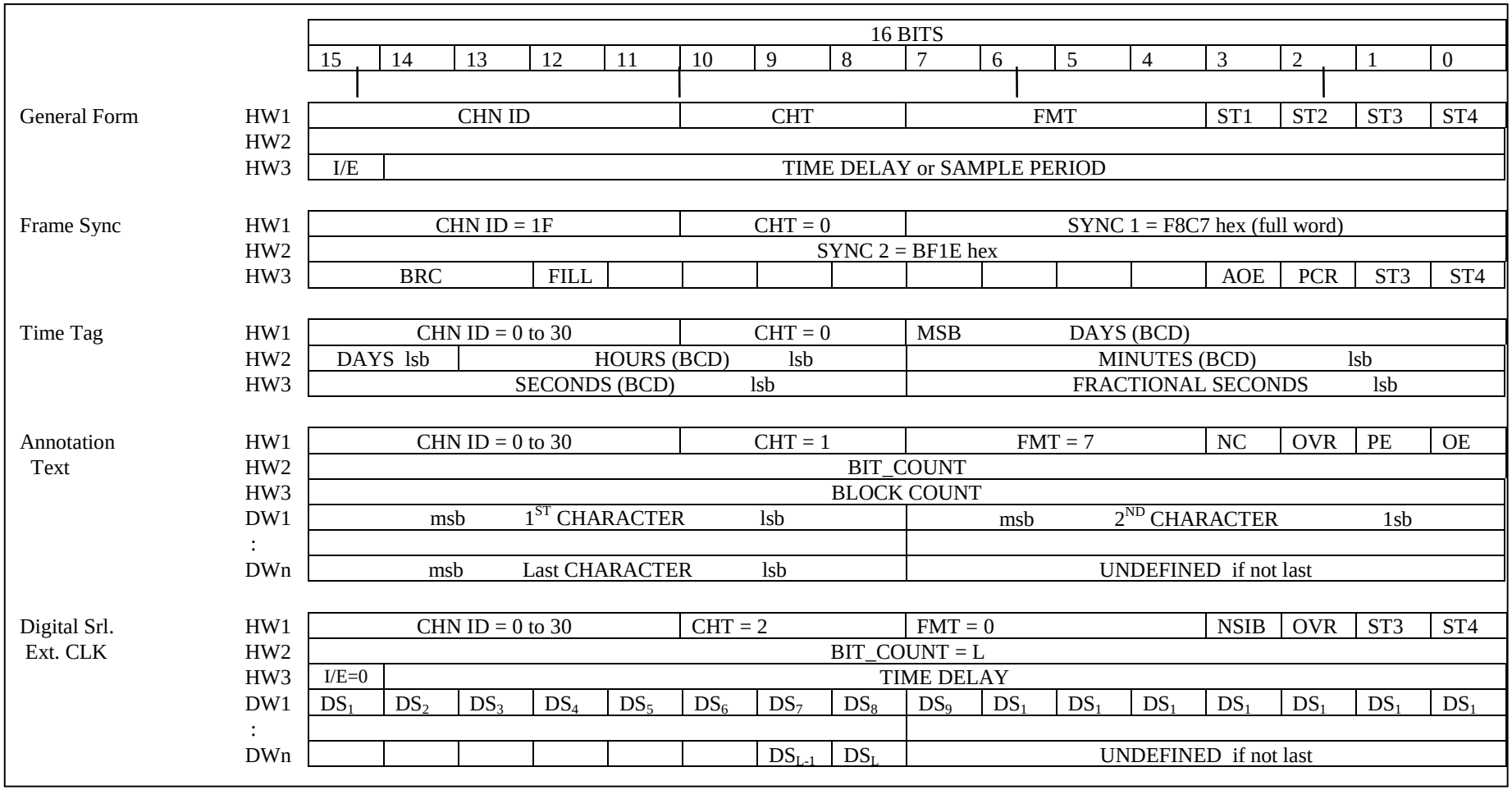


Figure G-4a. Submux data format.

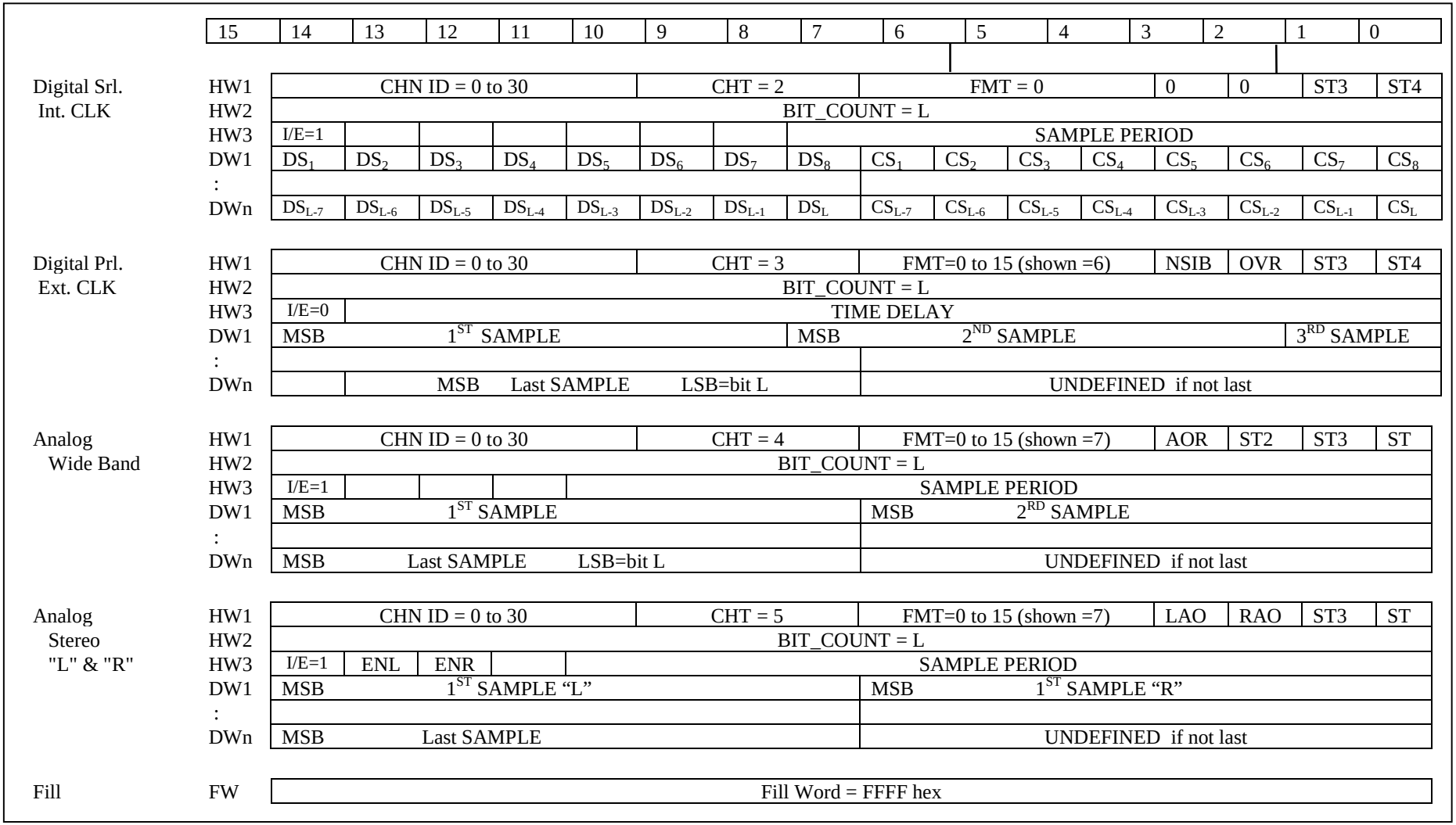


Figure G-4b. Submux data format.

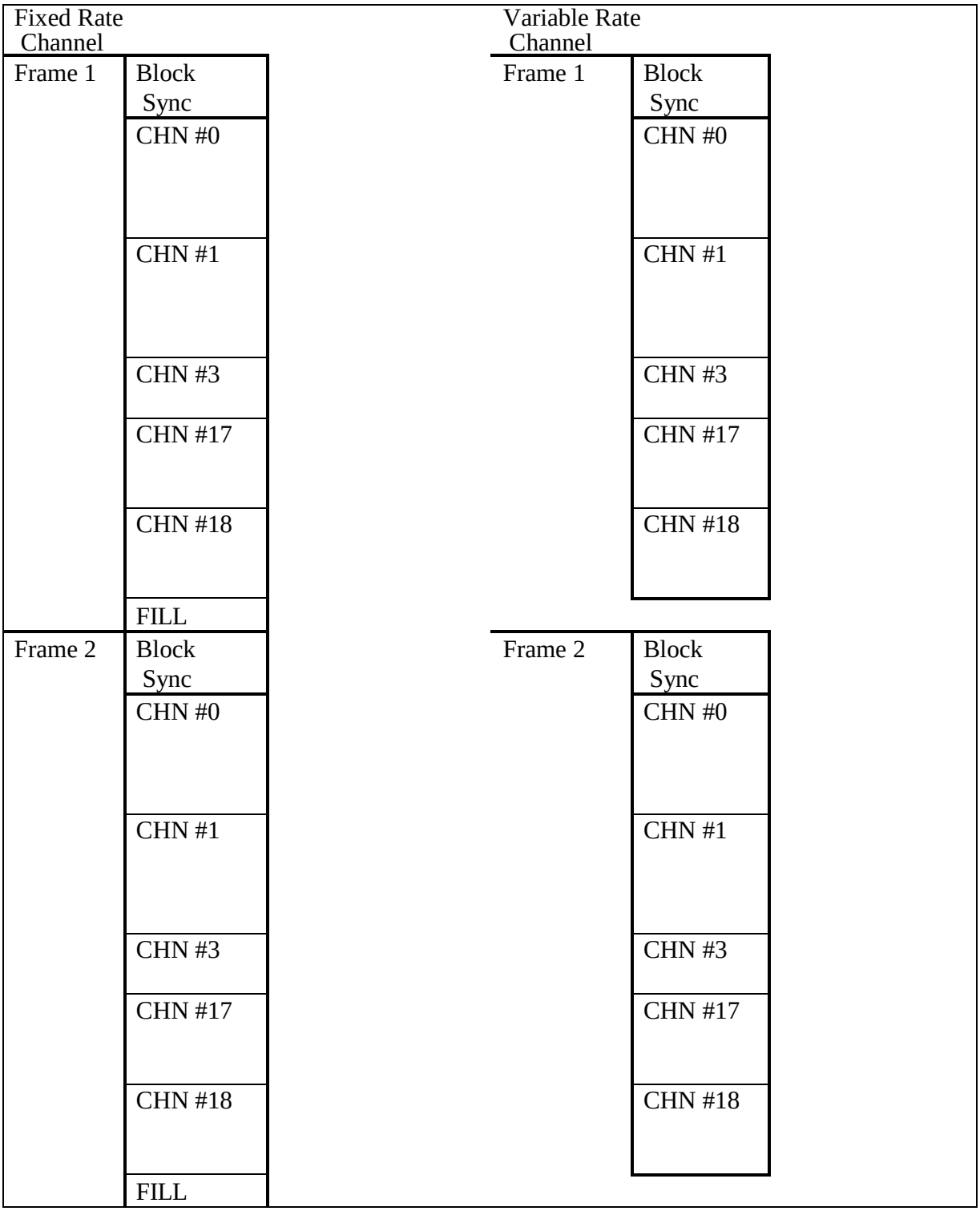


Figure G-5. Submux aggregate format.

APPENDIX H

APPLICATION OF THE TELEMETRY ATTRIBUTES TRANSFER STANDARD

APPENDIX H

APPLICATION OF THE TELEMETRY ATTRIBUTES TRANSFER STANDARD

Interchange of telemetry attributes occurs between vehicle instrumentation organizations (the source) and the telemetry ground stations (the destination). Interchange may also take place between ranges. The typical elements of this process are

- data entry system
- source data base
- export program
- interchange medium [this standard]
- import program
- destination data base
- telemetry setup system
- telemetry processing equipment

These elements are depicted in figure H-1 and are defined next.

1. The data entry system is the source organization's human interface where telemetry attributes are entered into a computer-based system. (Not affected by this standard.)

2. The source database is where telemetry attributes are maintained in a form appropriate to the local organization's needs. (Not affected by this standard.)

3. The export program converts the telemetry attributes from the source database format to the format defined by this standard and stores them on the interchange medium.

4. The interchange medium contains the telemetry attributes being transferred from the source organization to the destination organization. Format and contents are defined by this standard.

5. The import program reads the standardized interchange medium and converts the attributes to the destination data base format in accordance with local needs, system characteristics, and limitations.

6. The destination data base is where telemetry attributes are maintained in a form suitable to the local ground station's needs. (Not affected by this standard.)

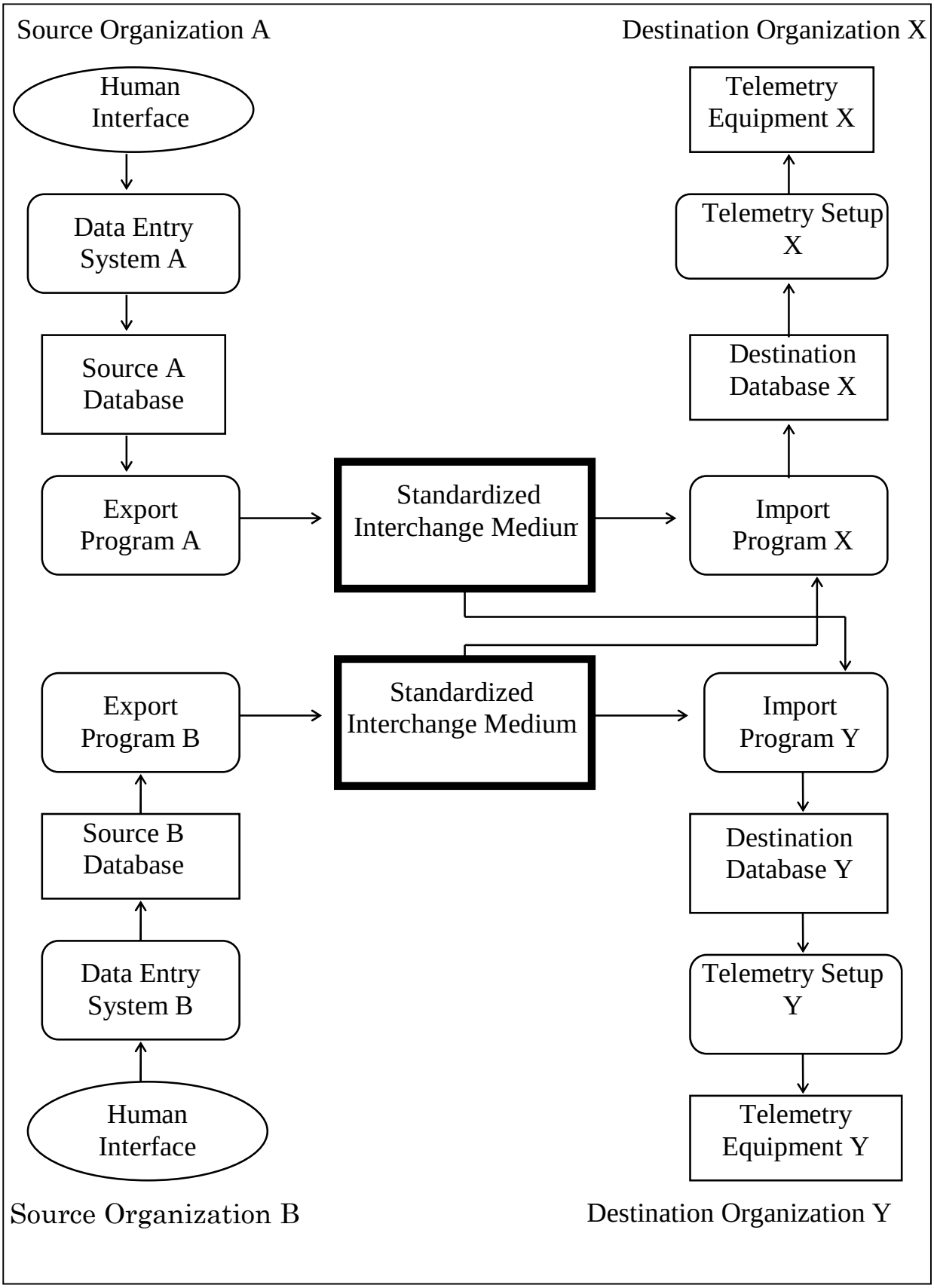


Figure H-1. Typical elements of the telemetry attributes transfer process.

7. The telemetry setup system accesses the destination database to load the telemetry processing equipment. (Not affected by this standard.)

8. The telemetry processing equipment is where the attributes will ultimately be used to properly handle the data being transmitted. (Not affected by this standard.)

The interchange medium is intended as a standard means of information exchange. The source and destination organizations are not constrained by this standard as to how the attributes are stored, viewed, used, or maintained.

To use the attribute transfer standard, import and export software must be developed. Once in place, these programs should eliminate the need for test item or project specific software at either the supplying (source) organizations or the processing (destination) organizations.

APPENDIX I

TELEMETRY ATTRIBUTES TRANSFER STANDARD COVER SHEET

APPENDIX I

TELEMETRY ATTRIBUTES TRANSFER STANDARD COVER SHEET

Each attribute transfer file (disk or tape) should be accompanied by a cover sheet describing the originating agency's computer system used to construct the attribute file. The recommended format for this cover sheet is given here.

Telemetry Measurement Attributes Transfer Standard

Date: MM\DD\YY

From: Name

Address

Telephone

To: Name

Address

Telephone

Originating computer system:

Computer make and model:

Medium characteristics:

Description:

Comments:

APPENDIX J

TELEMETRY ATTRIBUTES TRANSFER STANDARD FORMAT EXAMPLE

APPENDIX J

TELEMETRY ATTRIBUTES TRANSFER STANDARD FORMAT EXAMPLE

The following example is for illustrative purposes and is by no means a complete attributes file; it is representative of the types of information likely to be transferred. Many attributes are purposely omitted to simplify the example. In some of the groups, only those entries necessary to link to other groups are provided. Attributes, which link the various groups together, are indicated in **boldface**.

Selected attributes are described in text form as an aid to following the example. *All text, which describes the example, is printed in italics.* All text, which is part of the example file, is printed in plain text.

The example file being transferred consists of the attributes of a single RF data source and an analog tape containing two data sources. The RF data source is a PCM signal, which contains an embedded asynchronous wave train. The two recorded data sources are PCM signals: one is an aircraft telemetry stream, and the other is a radar data telemetry stream. Figure J-1 shows the example file in terms of the attribute groups and their interrelationships. Refer to the attribute tables while reviewing the example.

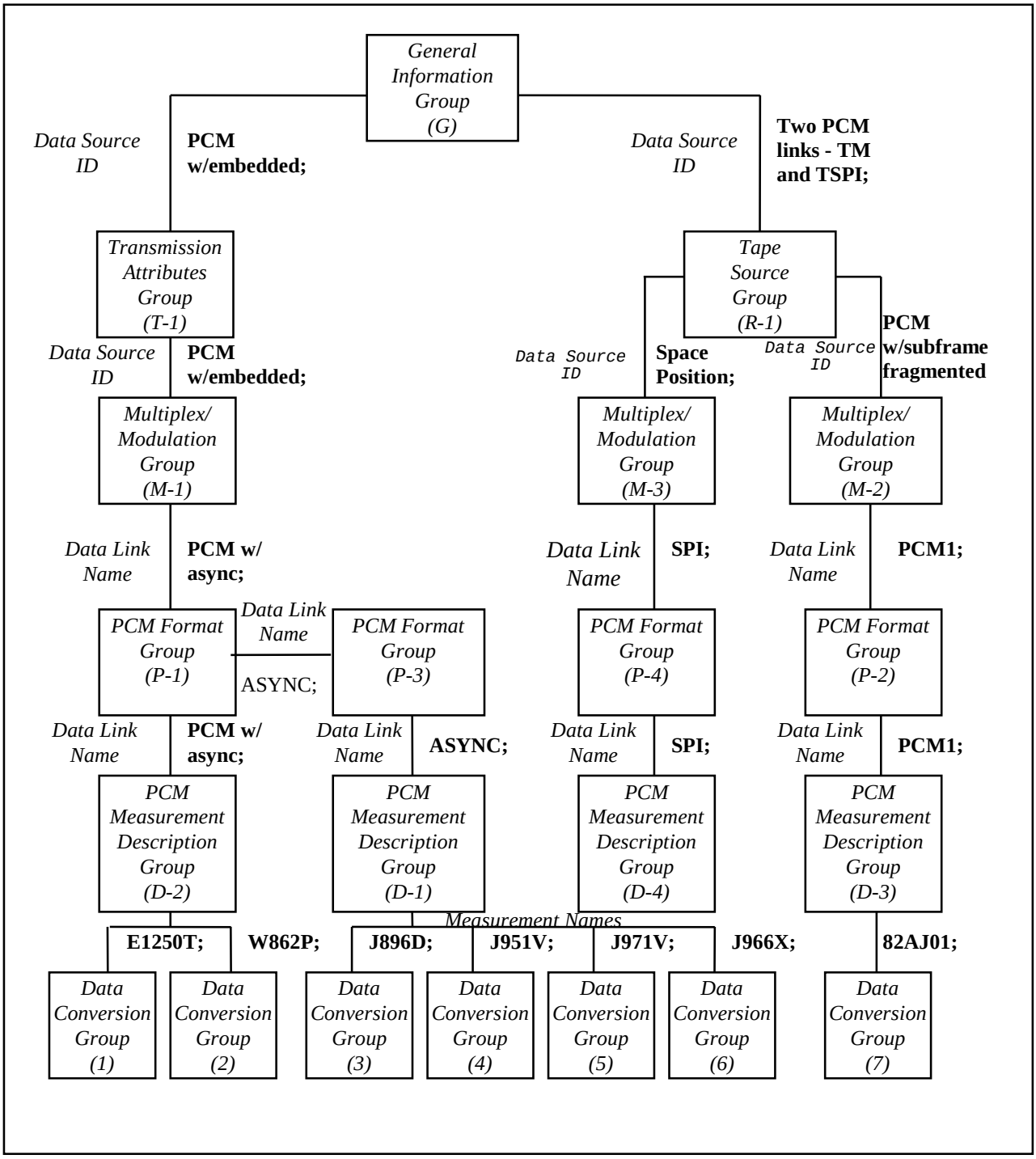


Figure J-1. Group linkages.

General Information Group (G)

Program name, test name, origination date, revision number: 0, test number: 13.

G\PN: TMATS example; G\TA: Wright Flyer; G\OD: 07-12-41; G\RN:0; G\TN:13;
G\POC1-1: Wilbur; G\POC2-1: Bikes,LTD; G\POC3-1: Dayton;
G\POC4-1: 555-1212;

Live data source.

G\DSI-1:PCM w/embedded; G\DST-1:RF;

Tape source.

G\DSI-2:Two PCM links - TM & TSPI; G\DST-2:TAP;
G\COM: I hope this flies.; G\POC1-2: Orville;
G\POC2-2:Bikes,LTD; G\POC3-2: Dayton; G\POC4-2: 555-1212;

Transmission Attributes Group (T-1)

Frequency: 1489.5, RF bandwidth: 100, data bandwidth: 100; not encrypted, modulation type: FM, total carrier modulation: 500, no subcarriers, transmit polarization: linear.

T-1\ID:PCM w/embedded; T-1\RF1:1489.5; T-1\RF2:100; T-1\RF3:100;
T-1\RF4:FM; T-1\RF5:500; T-1\SCO\N:NO; T-1\AN2:LIN; T-1\AP\POC1:
Pat Tern; T-1\AP\POC2:Transmissions,Inc.;
T-1\AP\POC3:Amityville,NY; T-1\AP\POC4:800-555-1212;

Tape Source Attributes Group (R-1)

R-1\ID:Two PCM links - TM & TSPI;
R-1\R1:Reel #1; R-1\TC1:ANAL; R-1\TC2:ACME; R-1\TC3:795;

Tape width: 1 inch, reel diameter: 14 inches, 14 tracks, record speed: 7.5 inches/second.

R-1\TC4:1.0; R-1\TC5:14.0; R-1\N:14; R-1\TC6:7.5;

Rewound: Yes, manufacturer: ZZ; model: 13, original: yes.

R-1\TC8:Y; R-1\RI1:ZZ; R-1\RI2:13; R-1\RI3:Y;
R-1\RI4:07-12-91-07-55-59; R-1\POC1:Mr. Reel; R-1\POC2:Tape Creations; R-1\POC3:Anywhere,Ttown; R-1\POC4:555-1212;

Track Number 2 contains aircraft telemetry PCM (w/subframe fragmented)

R-1\TK1-1:2; R-1\TK2-1:FM/FM;
R-1\DSI-1:PCM w/subframe fragmented; R-1\TK3-1:FWD;

Track Number 4 contains Space Position Information via PCM link

R-1\TK1-2:4; **R-1\DSI-2:Space Position Information;**

Multiplex/Modulation Groups (M-1, M-2, M-3)

Baseband type: PCM, modulation sense: POS, baseband data: PCM, low pass filter type: constant amplitude

M-1\ID:PCM w/embedded; M-1\BB1:PCM; M-1\BB2:POS; M-1\BSG1:PCM; M-1\BSF2:CA;
M-1\BB\DLN:PCM w/async;

M-2\ID:PCM w/subframe fragmented; M-2\BB\DLN:PCM1;

M-3\ID:Space Position; M-3\BB\DLN:SPI;

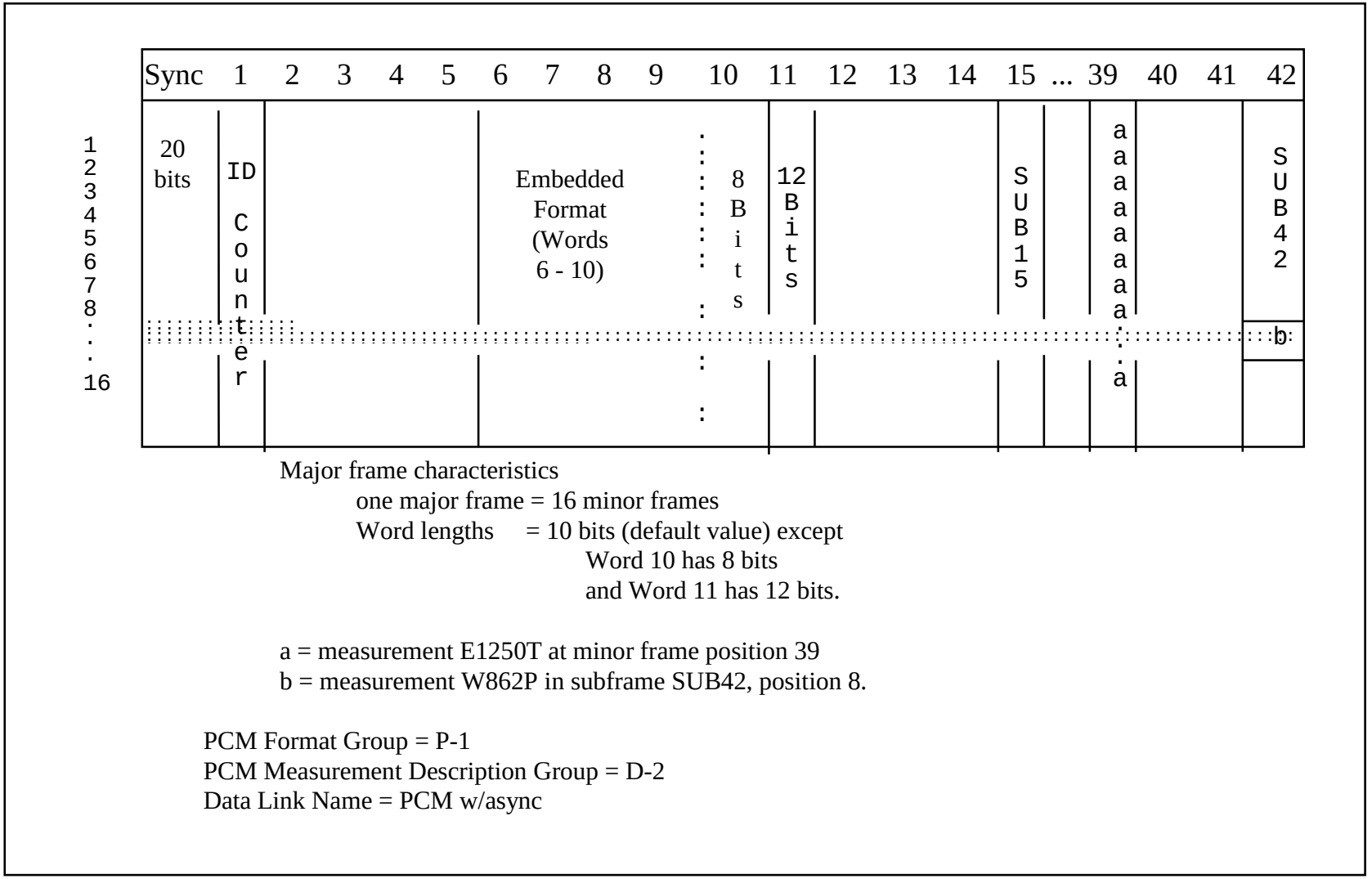
PCM Format Attributes Groups (P)

P-1 is a live PCM signal and contains the asynchronous wave train (see figure J-2).

P-2 is a recorded signal (see figure J-3).

P-3 is the asynchronous wave train (see figure J-4).

P-4 is a recorded signal.



Major frame characteristics

one major frame = 16 minor frames

Word lengths = 10 bits (default value) except
Word 10 has 8 bits
and Word 11 has 12 bits.

a = measurement E1250T at minor frame position 39

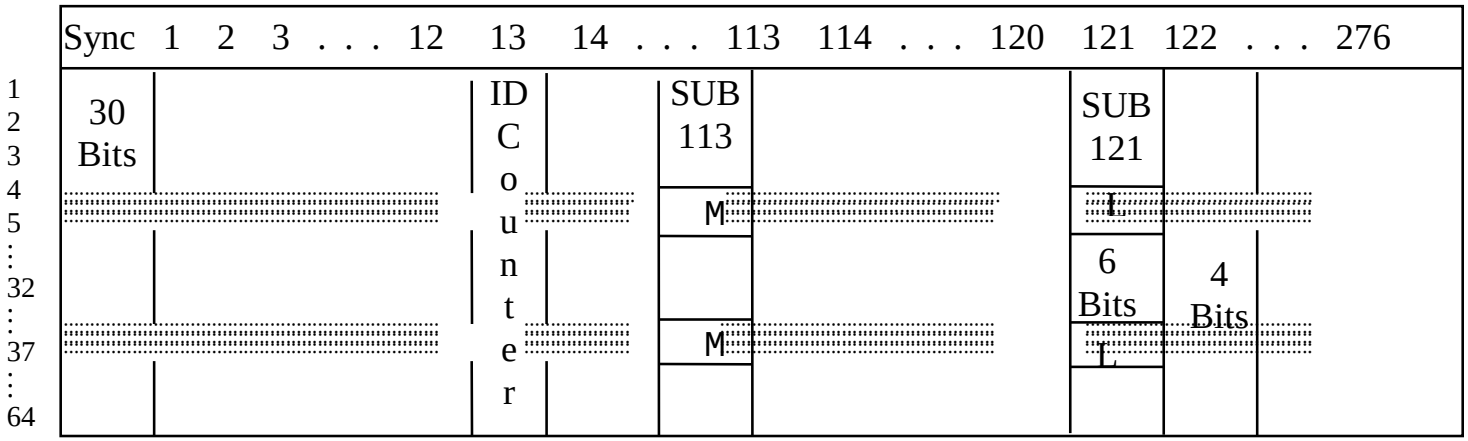
b = measurement W862P in subframe SUB42, position 8.

PCM Format Group = P-1

PCM Measurement Description Group = D-2

Data Link Name = PCM w/async

Figure J-2. PCM format for PCM w/async.



Major frame characteristics:

One major frame = 64 minor frames
Subframes SUB113 and SUB121 are 32 deep
ID counter counts 0 - 63
Word lengths = 10 (default value) except
Word 121 has 6 bits
and Word 122 has 4 bits.

Measurement 82AJ01 is 16 bits, which is fragmented with the 10 most significant bits indicated as M and the 6 least significant bits as L.
The measurement is located in position 5 of subframes SUB113 and SUB121 (minor frames 5 and 37 of the major frame).

PCM Format Group = P-2
PCM Measurement Description Group = D-3
Data Link Name = PCM1

Figure J-3. PCM format for PCM1.

	Sync	1	2	3	. . .	11	. . .	14	. . .	20	. . .	29	. . .	33	. . .	39	. . .	45	46	47	48	49
1	16 Bits	ID Counter	a	b	. .	a	. . .	c	. . .	a	. . .	a	. . .	a	. . .		. . .	ASUB2		a		
2			a	ASUB1	. .	a	. . .	ASUB3	. . .	a	. . .	a	. . .	a	. . .	cASUB3	. . .			a		
3			a		. .	a	. . .		. . .	a	. . .	a	. . .	a	. . .		. . .	d		a		

Major Frame characteristics
One major frame = 3 minor frames
Word lengths = 16 bits (default value)

a = measurement J971U, supercommutated at positions 2, 11, 20, 29, 33, and 47
b = measurement J951V in subframe ASUB1, position 1
c = measurement J896D in supercommutated subframe ASUB3, positions 1 and 4
d = measurement J966X in subframe ASUB2, position 3.

PCM Format Group = P-3
PCM Measurement Description Group = D-1
Data Link Name = ASYNC

Figure J-4. PCM format for async.

(Start of P-1)

Live PCM signal (host wave train) : Class I

P-1\DLN:PCM w/async; P-1\D1:NRZ-L; P-1\D2:44000; P-1\D3:U;
P-1\D4:N; P-1\D6:N; P-1\D7:N; P-1\TF:ONE;

10 bits default word length, 16 minor frames/major frame, 43 words/frame

P-1\F1:10; P-1\F2:M; P-1\F3:NO; P-1\MF\N:16; P-1\MF1:43;
P-1\MF2:440; P-1\MF3:FPT; P-1\MF4:20;
P-1\MF5: 01111010011010110001; P-1\SYNC1:1; P-1\SYNC2:0;
P-1\SYNC3:1;P-1\SYNC4:0;

Word position #10, 8 bits,
Word position #11, 12 bits

P-1\MFW1-1:10; P-1\MFW2-1:8; P-1\MFW1-2:11; P-1\MFW2-2:12;

One subframe ID counter

P-1\ISF\N:1; P-1\ISF1-1:1; P-1\ISF2-1:ID; P-1\IDC1-1:1;

ID counter word length : 10 bits,
MSB starting bit location : 7,
ID counter length : 4

P-1\IDC2-1:10; P-1\IDC3-1:7; P-1\IDC4-1:4; P-1\IDC5-1:M;
P-1\IDC6-1:0; P-1\IDC7-1:1; P-1\IDC8-1:15; P-1\IDC9-1:16;
P-1\IDC10-1:INC;

Subframe definition
SUB42 is located at 42, SUB15 at 15.
All have depth 16.

P-1\SF\N-1:2;

P-1\SF1-1-1:SUB42; P-1\SF2-1-1:NO;
P-1\SF4-1-1-1:42; P-1\SF6-1-1:16;
P-1\SF1-1-2:SUB15; P-1\SF2-1-2:NO;
P-1\SF4-1-2-1:15; P-1\SF6-1-2:16;

Asynchronous embedded wave train information

Data Link Name (to be referenced in the format definition of the asynchronous wave train) is ASYNC.

Five contiguous minor frame word positions starting at location 6.

P-1\AEF\N:1; **P-1\AEF\DLN-1:ASYNC;** P-1\AEF1-1:5; P-1\AEF2-1:CW; P-1\AEF3-1-1:6;

(End of P-1)

(Start of P-2)

Recorded PCM signal format attributes.

Data Link Name is PCM1, Data Format is NRZ-L, Bit rate is 2 Mbit/sec, Unencrypted, Normal polarity, class I, Common word length is 10, MSB first, No parity, 64 minor frames per major frame, 277 words per minor frame, Sync pattern length is 30. Word position 121 is 6 bits. Word position 122 is 4 bits.

P-2\DLN:PCM1;P-2\D1:NRZ-L; P-2\D2:2000000; P-2\D3:U; P-2\D4:N; P-2\TF:ONE; P-2\F1:10; P-2\F2:M; P-2\F3:NO; P-2\MF\N:64; P-2\MF1:277; P-2\MF4:30; P-2\MF5:10111000000110011111010110101 1; P-2\SYNC1:1; P-2\MFW1-1:121; P-2\MFW2-1:6; P-2\MFW1-2:122; P-2\MFW2-2:4;

Subframe characteristics:

One subframe ID counter named 1. Sync type is ID counter. ID counter location is 13. ID counter word length is 10. ID counter MSB location is 5. ID counter length is 6. ID counter transfer order is MSB first. ID counter initial value is 0. ID counter initial subframe is 1. ID counter end value is 63. ID counter end subframe is 64. ID counter is increasing.

Two subframes. First subframe name is SUB121. Not supercommutated, subframe location = word position 121, depth = 32. Second subframe name is SUB113. Not supercommutated, location = 113, depth = 32.

P-2\ISF\N:1; P-2\ISF1-1:1; P-2\ISF2-1:ID; P-2\IDC1-1:13;
P-2\IDC2-1:10; P-2\IDC3-1:5; P-2\IDC4-1:6; P-2\IDC5-1:M;
P-2\IDC6-1:0; P-2\IDC7-1:1; P-2\IDC8-1:63; P-2\IDC9-1:64;
P-2\IDC10-1:INC; P-2\SF\N-1:2; P-2\SF1-1-1:SUB121;
P-2\SF2-1-1:NO; P-2\SF4-1-1-1:121; P-2\SF6-1-1:32;
P-2\SF1-1-2:SUB113; P-2\SF2-1-2:NO; P-2\SF4-1-2-1:113;
P-2\SF6-1-2:32;

(End of P-2)

(Start of P-3)

Asynchronous wave train PCM format attributes.

Data Link Name: ASYNC
Class I, Common word length : 16, LSB transfer order, no parity
3 minor frames per major frame, 50 words/minor frame, 800 bits per minor frame, fixed pattern synchronization, 16 bit syncpattern.

P-3\DLN:ASYNC; P-3\TF:ONE; P-3\F1:16; P-3\F2:L; P-3\F3:NO;
P-3\MF\N:3; P-3\MF1:50; P-3\MF2:800; P-3\MF3:FPT; P-3\MF4:16;
P-3\MF5: 1111100110110001; P-3\SYNC1:1;

Subframe definition.

Three subframes with ID counter word length 16 at word position 1.

P-3\ISF\N:1; P-3\ISF1-1:2; P-3\ISF2-1:ID; P-3\IDC1-1:1;
P-3\IDC2-1:16; P-3\IDC3-1:15; P-3\IDC4-1:2; P-3\IDC5-1:L;
P-3\IDC6-1:0; P-3\IDC7-1:1; P-3\IDC8-1:2; P-3\IDC9-1:3;
P-3\IDC10-1:INC;

ASUB1 is at word position 3.
ASUB2 is at word position 45.
ASUB3 is supercommutated at word positions 14 and 39.

P-3\SF\N-1:3; P-3\SF1-1-1:ASUB1; P-3\SF2-1-1:NO; P-3\SF3-1-1:NA;
P-3\SF4-1-1-1:3; P-3\SF6-1-1:3; P-3\SF1-1-2:ASUB2;
P-3\SF2-1-2:NO; P-3\SF3-1-2:NA; P-3\SF4-1-2-1:45; P-3\SF6-1-2:3;
P-3\SF1-1-3:ASUB3; P-3\SF2-1-3:2; P-3\SF3-1-3:EL;
P-3\SF4-1-3-1:14; P-3\SF4-1-3-2:39; P-3\SF6-1-3:3;

(End of P-3)

(Start of P-4)

P-4\DLN:SPI;

(End of P-4)

PCM Measurement Description (D)

D-1 contains the measurements which make up the asynchronous wave train,

D-2 contains the measurements which make up the live PCM signal (which hosts the asynchronous wave train),

D-3 contains the measurements which make up one of the recorded PCM signals, and

D-4 contains the measurements which make up the other recorded PCM signal.

(Start of D-1)

Asynchronous Wave Train: One measurement list, 4 measurements

D-1\DLN:ASYNC; D-1\ML\N:1; D-1\MLN-1:JUST ONE; D-1\MN\N-1:4;

Measurement Name : J896D, LSB first,
Subframe supercommutated, 2 locations: 1 and 4 of ASUB3.

D-1\MN-1-1:J896D; D-1\MN3-1-1:L; D-1\LT-1-1:SFSC;
D-1\SFS1-1-1:ASUB3; D-1\SFS\N-1-1:2; D-1\SFS2-1-1:E;
D-1\SFS6-1-1-1:1; D-1\SFS6-1-1-2:4; D-1\SFS7-1-1-1:FW;
D-1\SFS7-1-1-2:FW;

Measurement Name: J951V, LSB first, default parity, subframe ASUB1, location 1.

D-1\MN-1-2:J951V; D-1\MN1-1-2:DE; D-1\MN2-1-2:D; D-1\MN3-1-2:L; D-1\LT-1-2:SF; D-1\SF2-1-2:1; D-1\SFM-1-2:1111111100000000;
D-1\SF1-1-2:ASUB1;

Measurement Name : J971U, LSB first,
supercommutated at positions 2, 11, 20, 29, 33, and 47.

D-1\MN-1-3:J971U; D-1\MN1-1-3:DE; D-1\MN2-1-3:D; D-1\MN3-1-3:L;
D-1\LT-1-3:MFSC; D-1\MFS\N-1-3:6; D-1\MFS1-1-3:E;
D-1\MFSW-1-3-1:2; D-1\MFSW-1-3-2:11; D-1\MFSW-1-3-3:20;
D-1\MFSW-1-3-4:29; D-1\MFSW-1-3-5:33; D-1\MFSW-1-3-6:47;

Measurement Name : J966X, LSB first, subframe ASUB2,
location 3.

D-1\MN-1-4:J966X; D-1\MN1-1-4:DE; D-1\MN2-1-4:D;
D-1\MN3-1-4:L; D-1\LT-1-4:SF; D-1\SF1-1-4:ASUB2;
D-1\SF2-1-4:3; D-1\SFM-1-4:FW;

(End of D-1)

(Start of D-2)

Live PCM signal: single measurement list, 2 measurements.

D-2\DLN:PCM w/async; D-2\MLN-1:JUST ONE; D-2\MN\N-1:2;

Measurement name: E1250T, unclassified, unsigned, MSB first.

D-2\MN-1-1:E1250T; D-2\MN1-1-1:DE; D-2\MN2-1-1:D;
D-2\MN3-1-1:M; D-2\LT-1-1:MF; D-2\MF-1-1:39; D-2\MFM-1-1:FW;

Measurement name: W862P, unclassified, MSB first,
subframe name: SUB42, location 8 in subframe, full word.

D-2\MN-1-2:W862P; D-2\MN1-1-2:DE; D-2\MN2-1-2:D; D-2\MN3-1-2:M; D-2\LT-1-2:SF; D-2\SF1-1-2:SUB42; D-2\SF2-1-2:8; D-2\SFM-1-2:FW;

(End of D-2)

(Start of D-3)

Recorded PCM signal: single measurement list: 1 measurement.

D-3\DLN:PCM1; D-3\MLN-1:ONLY ONE; D-3\MN\\N-1:1;

Measurement name: 82AJ01, subframe fragmented, 2 fragments, subframes: SUB113 and SUB121, subframe location: 5.

D-3\MN-1-1:82AJ01; D-3\LT-1-1:SFFR; D-3\FSF\N-1-1:2; D-3\FSF1-1-1:16; D-3\FSF2\N-1-1:2; D-3\FSF3-1-1-1:SUB113; D-3\FSF3-1-1-2:SUB121; D-3\FSF4-1-1-1:E; D-3\FSF8-1-1-1-1:5;

(End of D-3)

(Start of D-4)

Recorded PCM signal

D-4\DLN:SPI;

(End of D-4)

Data Conversion Groups (C)

C-1 and C-2 are measurements which are part of the live PCM signal (see also D-2).

C-3, C-4, C-5, and C-6 are from the asynchronous wave train (see also D-1).

C-7 is from the recorded PCM signal (see also D-3).

Measurement: E1250T, description: Inlet Temp Bellmouth, units: Deg C, binary format: unsigned; high value: 128, low value: -0.4,
conversion type: pair sets, number of pair sets: 2, application (polynomial) : Yes; order of fit: 1,
telemetry value #1: 0, engineering unit value #1: -0.4,
telemetry value #2: 1023, engineering unit value #2: 128.

C-1\DCN:E1250T; C-1\MN1:Inlet Temp Bellmouth; C-1\MN3:DEGC; C-1\BFM:UNS; C-1\MOT1:128; C-1\MOT2:-0.4; C-1\DCT:PRS; C-1\PS\N:2; C-1\PS1:Y; C-1\PS2:1; C-1\PS3-1:0; C-1\PS4-1:-0.4; C-1\PS3-2:1023; C-1\PS4-2:128;

Measurement: W862P, description: Fuel Pump Inlet, binary format: unsigned; conversion type: pair sets, number of pair sets: 2, application (polynomial): Yes; order of fit: 1, telemetry value #1: 0, engineering unit value #1: -0.1 telemetry value #2: 1023, engineering unit value #2: 76.7

C-2\DCN:W862P; C-2\MN1:Fuel Pump Inlet; C-2\BFM:UNS; C-2\DCT:PRS; C-2\PS\N:2; C-2\PS1:Y; C-2\PS2:1; C-2\PS3-1:0; C-2\PS4-1:-0.1; C-2\PS3-2:1023; C-2\PS4-2:76.7;

Measurement: J896D, description: Terrian Altitude, units: Feet, binary format: two's complement; high value: 32768, low value: -32768, conversion type: pair sets; number of pair sets: 2, application (polynomial): Yes, order of fit: 1, telemetry value #1: -32768, engineering unit value #1: -32768, telemetry value #2: 32767, engineering unit value #2: 32767

C-3\DCN:J896D; C-3\MN1:Terrian Altitude; C-3\MN3:FEET; C-3\BFM:TWO; C-3\MOT1:32768; C-3\MOT2:-32768; C-3\DCT:PRS; C-3\PS\N:2; C-3\PS1:Y; C-3\PS2:1; C-3\PS3-1:-32768; C-3\PS4-1:-32768; C-3\PS3-2:32767; C-3\PS4-2:32767;

Measurement: J951V, description: Throttle Command, units: VDC, high value: 10.164, low value: -10.164, conversion type: pair sets, number of pair sets: 2, application(polynomial): Yes, order of fit: 1, telemetry value #1: -128, engineering unit value #1: -10.164, telemetry value #2: 127, engineering unit value #2: 10.164 binary format: two's complement;

C-4\DCN:J951V; C-4\MN1:Throttle Command; C-4\MN3:VDC; C-4\MOT1:10.164; C-4\MOT2:-10.164; C-4\DCT:PRS; C-4\PS\N:2; C-4\PS1:Y; C-4\PS2:1; C-4\PS3-1:-128; C-4\PS4-1:-10.164; C-4\PS3-2:127; C-4\PS4-2:10.164; C-4\BFM:TWO;

Measurement: J971U; description: DISC, conversion type: discrete, binary format: unsigned.

C-5\DCN:J971U; C-5\MN1:DISC; C-5\DCT:DIS; C-5\BFM:UNS;

Measurement: J966X; description: Discrete, conversion type: discrete, binary format: unsigned.

C-6\DCN:J966X; C-6\MN1:Discrete; C-6\DCT:DIS; C-6\BFM: UNS;

Measurement: 82AJ01, description: LANTZ Norm acceleration, units: MTR/S/S, High value: 1023.97, Low value: -1023.97, conversion type: Coefficients
Order of curve fit: 1, derived from pair sets: No,
Coefficient (0): 0, Coefficient(1): 0.03125, binary format: two's complement

C-7\DCN:82AJ01; C-7\MN1:LANTZ Norm acceleration; C-7\MN3:MTR/S/S; C-7\MOT1:1023.97; C-7\MOT2:-1023.97; C-7\DCT:COE; C-7\CO\N:1; C-7\CO1:N; C-7\CO:0; C-7\CO-1:.03125; C-7\BFM:TWO;

APPENDIX K

PULSE AMPLITUDE MODULATION STANDARDS

APPENDIX K

PULSE AMPLITUDE MODULATION STANDARDS

1.0 General

This standard defines the recommended pulse train structure and design characteristics for the implementation of PAM telemetry systems. The PAM data are transmitted as time division multiplexed analog pulses with the amplitude of the information channel pulse being the analog- variable parameter.

2.0 Frame and Pulse Structure

Each frame consists of a constant number of time-sequenced channel intervals. The maximum frame length shall be 128 channel time intervals per frame, including the intervals devoted to synchronization and calibration. The pulse and frame structure shall conform to either figure K-1 or K-2.

2.1.1 Commutation Pattern. The information channels are allocated equal and constant time intervals within the PAM frame. Each interval ("T" in figures K-1 and K-2) contains a sample pulse beginning at the start of the interval and having amplitude determined by the amplitude of the measurand of the corresponding information channel according to a fixed relationship (usually linear) between the minimum level (zero amplitude) and the maximum level (full-scale amplitude). For a 50-percent duty cycle (RZ-PAM), the zero level shall be 20 to 25 percent of the full amplitude level as shown in figure K-1. The pulse width shall be the same in all time intervals except for the intervals devoted to synchronization. The duration shall be either 0.5T ±0.05, as shown in figure K-1, or T ±0.05, as shown in figure 5-2.

2.1.2 In-Flight Calibration. It is recommended that in-flight calibration be used and channels 1 and 2, immediately following the frame synchroniza-tion interval, be used for zero and full-scale calibration. For RZ-PAM, channel 3 may be used for an optional half-scale calibration, and for NRZ-PAM, the channel interval preceding channel 1 may be used for half-scale calibration if set to 50 percent.

2.1.3 Frame Synchronization Interval. Each frame is identified by the presence within it of a synchronization interval.

2.1.3.1 Fifty Percent Duty Cycle (RZ-PAM). The synchronization pattern interval shall have a duration equal to two information channel intervals (2T) and shall be full-scale amplitude for 1.5T followed by the reference level or zero baseline for 0.5T (see figure K-1).

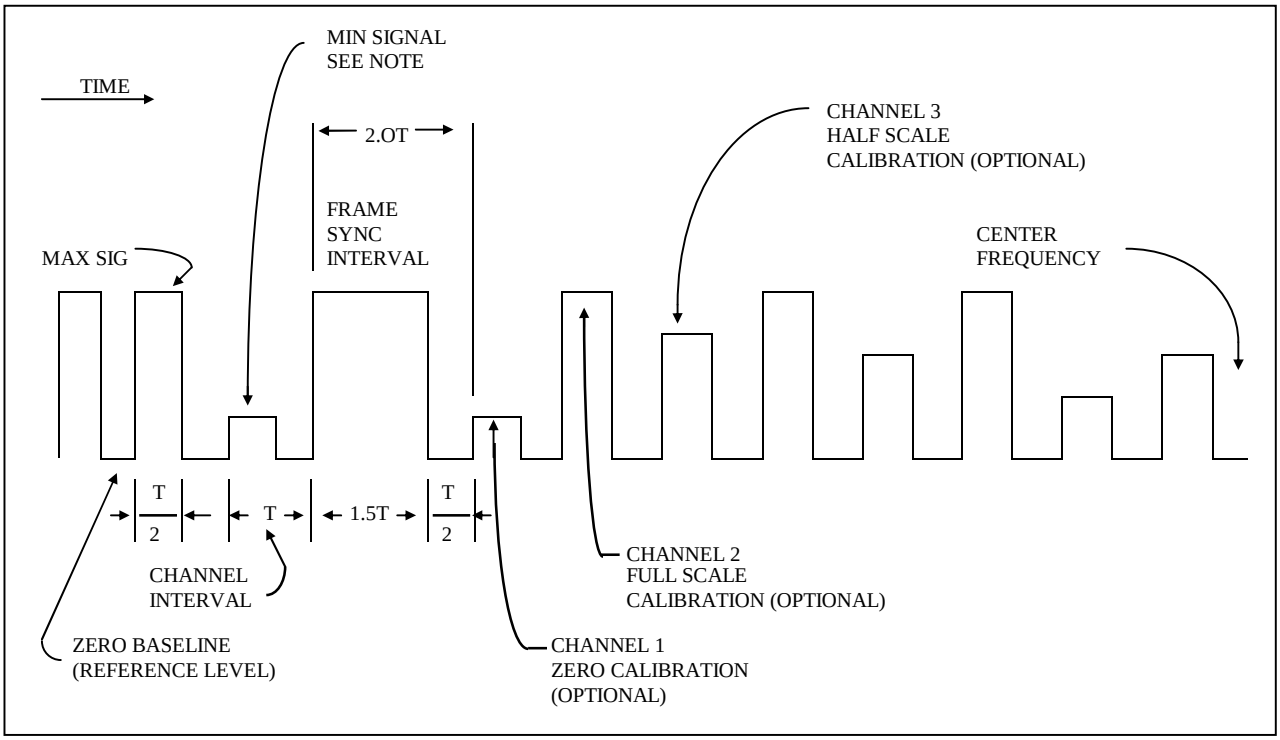


Figure K-1. 50-percent duty cycle PAM with amplitude synchronization.

NOTE A 20 to 25 percent deviation reserved for pulse synchronization is recommended.

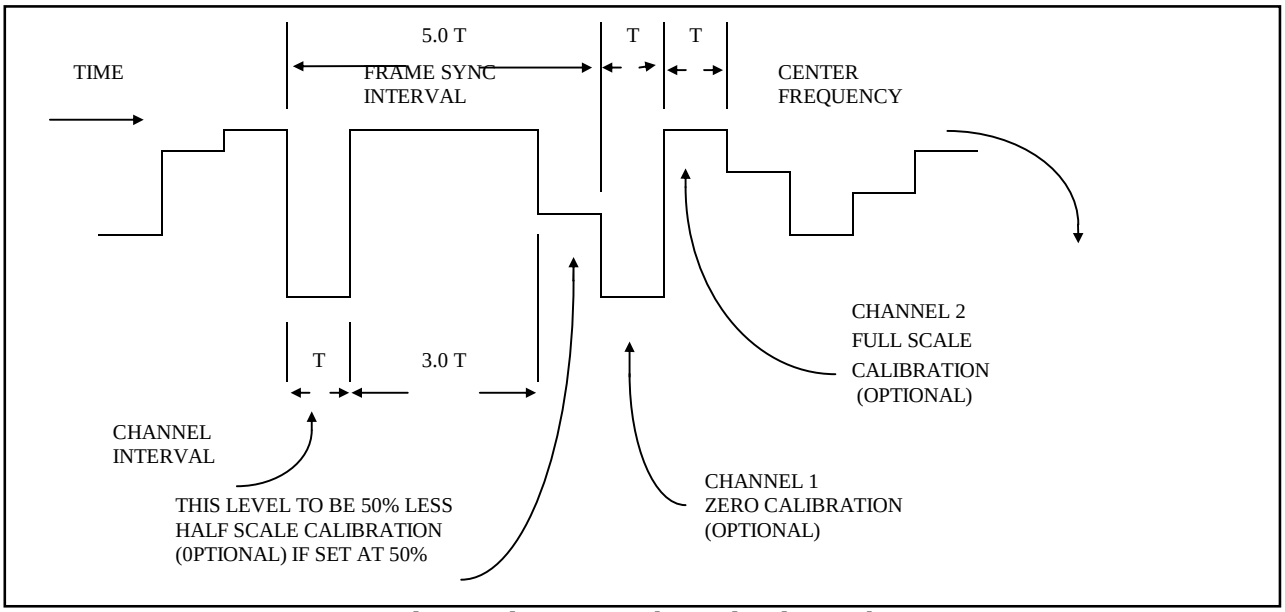


Figure K-2. 100-percent duty cycle PAM with amplitude synchronization.

2.1.3.2 One Hundred Percent Duty Cycle (NRZ-PAM). The synchronization pattern is in the order given: zero level for a period of T, full-scale amplitude for a period of 3T, and a level not exceeding 50-percent full-scale amplitude for a period T (see figure K-2).

2.1.4 Maximum Pulse Rate. The maximum pulse rate should not be greater than that permitted by the following subparagraphs.

2.1.4.1 PAM/FM/FM. The reciprocal of the shortest interval between transitions in the PAM pulse train shall not be greater than one-fifth of the total (peak-to-peak) deviation specified in chapter 3 and tables 3-1 and 3-2 for the FM subcarrier selected.

2.1.4.2 PAM/FM. The reciprocal of the shortest interval between transitions in the PAM pulse train shall be limited by whichever is the narrower of the following:

2.1.4.2.1 One-half of the 3 dB frequency of the premodulation filter when employed.

2.1.4.2.2 One-fifth of the intermediate frequency (IF) bandwidth (3 dB points) selected from the IF bandwidths which are listed in table 2-1.

2.2 Frame and Pulse Rate. The frame and pulse parameters listed below may be used in any combination:

- a minimum rate of 0.125 frames per second, and
- a maximum pulse rate as specified in subparagraph 2.1.4.

2.2.1 Long Term Accuracy and Stability. During a measured period of desired data, the time between the occurrence of corresponding points in any two successive frame synchronization intervals should not differ from the reciprocal of the specified nominal frame rate by more than 5 percent of the nominal period.

2.2.2 Short Term Stability. During a measured period, P, containing 1000-channel intervals, the time between the start of any two successive channel intervals (synchronization intervals excepted) should not differ from the average channel interval established by the formula $T_{avg} = \frac{P}{1000}$ by more than 1 percent of the average interval

2.3 Multiple and Submultiple Sampling Rates. Data multiplexing at sampling rates which are multiples and submultiples of the frame rate is permissible.

2.3.1 Submultiple Frame Synchronization. The beginning of the longest submultiple frame interval is identified by the transmission of a synchronization pattern. All other submultiple frames have a fixed and known relationship to the identified submultiple frames.

2.3.1.1 Fifty Percent Duty Cycle (RZ). The synchronization pattern has a full-scale amplitude pulse in two successive occurrences of channel intervals allocated to data channels of the identified submultiple frame. The first such pulse has a duration equal to the channel interval; the second pulse immediately follows the first pulse and has a duration nominally one-half the channel interval. There is no return to zero between the two pulses.

2.3.1.2 One Hundred Percent Duty Cycle (NRZ). The synchronization pattern has information in five successive occurrences of a channel interval allocated to data channels of the identified submultiple frame. The amplitude of the data channels assigned for synchronization is shown in the following subparagraphs.

2.3.1.2.1 First occurrence - zero amplitude.

2.3.1.2.2 Second, third, and fourth occurrences - full-scale amplitude.

2.3.1.2.3 Fifth occurrence - not more than 50 percent of full-scale amplitude.

2.3.2 Maximum Submultiple Frame Length. The interval of any submultiple frame, including the time devoted to synchronizing information, shall not exceed 128 times the interval of the frame in which it occupies a recurring position.

2.4 Frequency Modulation. The frequency deviation of an FM carrier or subcarrier, which represents the maximum and minimum amplitude of a PAM waveform, should be equal and opposite with respect to the assigned carrier or subcarrier frequency. The deviation should be the same for all occurrences of the same level.

2.5 Premodulation Filtering. A maximally linear phase response, premodulation filter, is recommended to restrict the radiated spectrum (see appendix A).

APPENDIX L

ARMOR

APPENDIX L

ARMOR

1.0 General

This standard defines the recommended multiplexer format for single channel data recording on small format (1/2") media (reference 6.17). This format is recognized as the Asynchronous Recorder Multiplexer Output Re-constructor (ARMOR). This format is software-reconfigurable for each data acquisition or reproduction. The ARMOR format configuration information is stored in a data structure called a "setup" that contains all the information necessary to define a particular record or play configuration. This appendix describes the format and content of the ARMOR setup.

1.1 Setup on Tape. When the ARMOR setup is written to tape, it is preceded by a preamble with a unique setup sync pattern that allows the identification of the setup. Three duplicate setup records, each with its own preamble, are written at the beginning of each recording. The format of the preamble is defined in Table L-1.

TABLE L-1. ARMOR SETUP PREAMBLE

FIELD	LENGTH	DESCRIPTION
SETUP SYNC	4 TAPE BLOCKS	THE SYNC PATTERN CONSISTS OF TWO BYTES. THE HIGH BYTE IS 0XE7; THE LOW BYTE IS 0X3D. THE SYNC PATTERN IS WRITTEN HIGH BYTE FIST. FOR THE DCRSI, A TAPE BLOCK IS A SINGLE SCAN (4356 BYTES). FOR THE VLDS, A TAPE BLOCK IS A PRINCIPLE BLOCK (65536 BYTES).
END OF SYNC	3 BYTES	THE THREE BYTES IMMEDIATELY FOLLOWING THE SYNC PATTERN ARE: 0X45, 0X4F, 0X53 (ASCII 'E', 'O', 'S' FOR "END OF SYNC").

2.0 Setup Organization

An ARMOR setup is divided into three sections: the header section, the channel section, and the trailer section. The overall organization of a setup is summarized in Table L-2.

TABLE L-2. SETUP ORGANIZATION

CONTENT	NUMBER OF BYTES
HEADER SECTION	70
CHANNEL 1 INFORMATION	51 - 61
CHANNEL 2 INFORMATION	51 - 61
"	"
"	"
TRAILER SECTION	0 - 44 + SAVED SCANLIST SIZE

2.1 Header Section The header section is the first 70 bytes of a setup. It contains information about the setup as a whole, including clock parameters, frame parameters, and the numbers of input and output channels (see Table L-3).

In tables L-3 through L-12, fields noted with an asterisk (*) require user input per section 2.5.

TABLE L-3. HEADER SECTION FORMAT			
FIELD	**BYTES**	**FORMAT**	**DESCRIPTION**
*SETUP LENGTH	2	BINARY	TOTAL BYTES IN SETUP, INCLUDING THIS FIELD.
SOFTWARE VERSION	12	ASCII	VERSION OF THE ARMOR SETUP AND CONTROL SOFTWARE THAT WROTE THE SETUP.
PRE-SCALERS	1	BINARY	THE BOTTOM FOUR BITS CONTAIN THE BIT RATE CLOCK PRE-SCALER; THE TOP FOUR BITS CONTAIN THE PACER CLOCK PRE-SCALER
RESERVED	26	N/A	N/A
*SETUP KEYS (BIT 0)	1	BINARY	IF BIT 0 (LSB) SET, SETUP CONTAINS SETUP DESCRIPTION IN TRAILER.
*SETUP KEYS (BITS 1, 2, & 3)			IF BIT 1 SET, SETUP CONTAINS CHECKSUM IN TRAILER. IF BIT 2 SET, SETUP IS SCAN-ALIGNED. IF BIT THREE SET THEN A SCAN LIST IS SAVED.
PACER DIVIDER	2	BINARY	PACER DIVIDER VALUE.
BIT RATE	4	BINARY	AGGREGATE BIT RATE FOR ALL ENABLED CHANNELS.
BRC DIVIDER	2	BINARY	BIT RATE CLOCK DIVIDER VALUE.
MASTER OSCILLATOR	4	BINARY	FREQUENCY OF THE MASTER OSCILLATOR IN BITS PER SECOND.
BYTES OVERHEAD	4	BINARY	TOTAL SYNC BYTES PLUS FILLER BYTES PER FRAME.
PACER	4	BINARY	FREQUENCY OF THE PACER CLOCK IN CYCLES PER SECOND.
FRAME RATE	4	BINARY	NUMBER OF FRAMES PER SECOND.
*INPUT COUNT	2	BINARY	NUMBER OF INPUT CHANNELS IN SETUP.
OUTPUT COUNT	2	BINARY	NUMBER OF OUTPUT CHANNELS IN SETUP.

2.2 Channel Section. The Channel section contains one channel entry for every channel in the multiplexer chassis configuration, including those channels that are not enabled or recorded. The content and length of the channel information vary depending on the channel type. The lengths of the channel entries for each channel type are presented in Table L-4. Tables L-5 through L-13 describe the channel entry fields for each module type.

TABLE L-4. CHANNEL ENTRY LENGTHS

CHANNEL TYPE	BYTES
PCM INPUT AND OUTPUT	51
ANALOG INPUT AND OUTPUT	53
PARALLEL INPUT	53
PARALLEL OUTPUT	56
TIMECODE INPUT AND OUTPUT	61
VOICE INPUT AND OUTPUT	61
BIT SYNC INPUT	61

TABLE L-5. PCM INPUT CHANNELS

FIELD	BYTES	FORMAT	DESCRIPTION
*CHANNEL TYPE	2	BINARY	1 = 8 BIT PCM INPUT 8 = 20 MBIT PCM INPUT
MAPPED CHANNEL	2	BINARY	INDEX OF THE CHANNEL THIS CHANNEL IS MAPPED TO. IF THE CHANNEL IS NOT MAPPED, THE INDEX IS -1.
*ENABLED	1	ASCII	IF ENABLED, THE CHANNEL IS RECORDED (“Y” OR “N”).
ACTUAL RATE	4	BINARY	ACTUAL WORD RATE IN WORDS PER SECOND.
WORDS PER FRAME	4	BINARY	NUMBER OF WORDS PER FRAME.
INPUT MODES	1	BINARY	IF BIT 0 (LSB) SET, SOURCE B DATA; ELSE SOURCE A. IF BIT 1 SET, NRZ-L; ELSE BIPHASE-L. IF BIT 2 SET, 0 DEGREE CLOCK; ELSE 90 DEGREE CLOCK.
RESERVED	3	N/A	N/A
BITS PER WORD	2	BINARY	16 BITS.
BITS PRECEDING	4	BINARY	NUMBER OF BITS IN THE FRAME THAT MUST PRECEDE THIS CHANNEL.
*CHANNEL NUMBER	2	BINARY	CHANNEL ON MODULE (0-3).
*MODULE ID	1	BINARY	MODULE ID = HEX 11
RESERVED	1	N/A	N/A
*REQUESTED RATE	4	BINARY	REQUESTED BITS PER SECOND (INTEGER).
DESCRIPTION	20	ASCII	CHANNEL DESCRIPTION.

TABLE L-6. ANALOG INPUT AND OUTPUT CHANNELS			
FIELD	**BYTES**	**FORMAT**	**DESCRIPTION**
CHANNEL TYPE	2	BINARY	2 = 8 MBIT PCM OUTPUT 9 = 20 MBIT PCM OUTPUT
MAPPED CHANNEL	2	BINARY	INDEX OF THE CHANNEL THIS CHANNEL IS MAPPED TO . IF THE CHANNEL IS NOT MAPPED, THE INDEX IS -1.
ENABLED	1	ASCII	IF ENABLED, THE CHANNEL IS RECORDED (“Y” OR “N”).
ACTUAL RATE	4	BINARY	ACTUAL WORD RATE IN WORDS PER SECOND.
WORDS PER FRAME	4	BINARY	NUMBER OF WORDS PER FRAME.
OUTPUT MODES	1	BINARY	IF BIT 0 (LSB) SET, BURST MODE. IF BIT 1 SET, BIPHASE; ELSE NRZ-L.
RESERVED	3	N/A	N/A
BITS PER WORD	2	BINARY	NUMBER OF BITS PER WORD.
BITS PRECEDING	4	BINARY	NUMBER OF BITS IN THE FRAME THAT MUST PRECEDE THIS CHANNEL.
CHANNEL NUMBER	2	BINARY	CHANNEL ON MODULE (0-3).
MODULE ID	1	BINARY	MODULE ID = HEX 21
RESERVED	1	N/A	N/A
REQUESTED RATE	4	BINARY	REQUESTED BITS PER SECOND.
DESCRIPTION	20	ASCII	CHANNEL DESCRIPTION.

TABLE L-7. ANALOG INPUT AND OUTPUT CHANNELS			
FIELD	**BYTES**	**FORMAT**	**DESCRIPTION**
*CHANNEL TYPE	2	BINARY	5 = LF ANALOG INPUT 6 = HF ANALOG INPUT 7 = ANALOG OUTPUT
MAPPED CHANNEL	2	BINARY	INDEX OF THE CHANNEL THIS CHANNEL IS MAPPED TO. IF THE CHANNEL IS NOT MAPPED, THE INDEX IS -1.
*ENABLED	1	ASCII	IF ENABLED, THE CHANNEL IS RECORDED (“Y” OR “N”).
ACTUAL RATE	4	BINARY	ACTUAL SAMPLE RATE IN SAMPLES PER SECOND.
SAMPLES PER FRAME	4	BINARY	NUMBER OR SAMPLES PER FRAME.
FILTER NUMBER	1	BINARY	0 = FILTER 1 1 = FILTER 2 2 = FILTER 3 3 = FILTER 4
RESERVED	3	N/A	N/A
*BITS PER SAMPLE	2	BINARY	NUMBER OF BITS PER SAMPLE (8 OR 12).
RESERVED	4	N/A	N/A
*CHANNEL NUMBER	2	BINARY	CHANNEL ON MODULE (0-3).
*MODULE ID	1	BINARY	MODULE ID = 34 HEX (LF) OR 33 HEX (HF)
RESERVED	1	N/A	N/A
*REQUESTED RATE	4	BINARY	REQUESTED SAMPLES PER SECOND.
RESERVED	2	N/A	N/A
DESCRIPTION	20	ASCII	CHANNEL DESCRIPTION

TABLE L-8. PARALLEL INPUT CHANNELS

FIELD	BYTES	FORMAT	DESCRIPTION
*CHANNEL TYPE	2	BINARY	13 = NEW PARALLEL INPUT
MAPPED CHANNEL	2	BINARY	INDEX OF THE CHANNEL THIS CHANNEL IS MAPPED TO. IF THE CHANNEL IS NOT MAPPED, THE INDEX IS -1.
*ENABLED	1	ASCII	IF ENABLED, THE CHANNEL IS RECORDED (“Y” OR “N”).
ACTUAL RATE	4	BINARY	ACTUAL WORDS PER SECOND.
WORDS PER FRAME	4	BINARY	NUMBER OF WORDS PER FRAME.
RESERVED	4	N/A	N/A
BITS PER WORD	2	BINARY	NUMBER OF BITS PER WORD
WORDS PRECEDING	4	BINARY	NUMBER OF WORDS IN THE FRAME THAT MUST PRECEDE THIS CHANNEL.
*CHANNEL NUMBER	2	BINARY	CHANNEL ON MODULE (0-3).
*MODULE ID	1	BINARY	MODULE ID = HEX 92
RESERVED	1	N/A	N/A
*REQUESTED RATE	4	BINARY	REQUESTED WORDS PER SECOND.
INPUT MODE	1	BINARY	0 = FOUR 8-BIT CHANNELS 1 = ONE 16-BIT, TWO 8-BIT (CURRENTLY UNAVAILABLE) 2 = TWO 16-BIT (CURRENTLY UNAVAILABLE) 3 = ONE 32-BIT (CURRENTLY UNAVAILABLE) 4 = ONE 24-BIT, ONE 8-BIT (CURRENTLY UNAVAILABLE)
RESERVED	1	N/A	N/A
DESCRIPTION	20	ASCII	CHANNEL DESCRIPTION.

TABLE L-9. PARALLEL OUTPUT CHANNELS			
FIELD	**BYTES**	**FORMAT**	**DESCRIPTION**
CHANNEL TYPE	2	BINARY	14 = NEW PARALLEL OUTPUT
MAPPED CHANNEL	2	BINARY	INDEX OF THE CHANNEL THIS CHANNEL IS MAPPED TO. IF THE CHANNEL IS NOT MAPPED, THE INDEX IS -1.
ENABLED	1	ASCII	IF ENABLED, THE CHANNEL IS RECORDED (“Y” OR “N”).
ACTUAL RATE	4	BINARY	ACTUAL WORD RATE IN WORDS PER SECOND.
WORDS PER FRAME	4	BINARY	NUMBER OF WORDS PER FRAME.
RESERVED	4	N/A	N/A
BITS PER WORD	2	BINARY	NUMBER OF BITS PER WORD.
WORDS PRECEDING	4	BINARY	NUMBER OF WORDS IN THE FRAME THAT MUST PRECEDE THIS CHANNEL.
CHANNEL NUMBER	2	BINARY	CHANNEL ON MODULE (0-3).
MODULE ID	1	BINARY	MODULE ID = HEX A2
RESERVED	1	N/A	N/A
REQUESTED RATE	4	BINARY	REQUESTED WORDS PER SECOND.
OUTPUT MODE	1	BINARY	0 = FOUR 8-BIT CHANNELS 1 = ONE 16-BIT, TWO 8-BIT 2 = TWO 16-BIT CHANNELS 3 = ONE 32-BIT CHANNEL 4 = ONE 24-BIT, ONE 8-BIT 7 = TWO 8-BIT DCRSI MODE
RECONSTRUCT MODE	1	BINARY	0 = DATA IS FROM MODULE OTHER THAN PARALLEL INPUT. 1 = DATA IS FROM PARALLEL INPUT. NOT VALID ONLY FOR OUTPUT MODE.
DCRSI OUTPUT	1	BINARY	0 = HEADER AND DATA 1 = HEADER ONLY 3 = DATA ONLY VALID ONLY FOR OUTPUT MODE 7.
BURST SELECT	1	BINARY	0 = CONSTANT 1 = BURST
HANDSHAKE SELECT	1	BINARY	0 = DISABLE HANDSHAKING 1 = ENABLE HANDSHAKING
DESCRIPTION	20	ASCII	CHANNEL DESCRIPTION.

TABLE L-10. TIME CODE INPUT CHANNELS			
FIELD	**BYTES**	**FORMAT**	**DESCRIPTION**
*CHANNEL TYPE	2	BINARY	TIME CODE MUST APPEAR AS A GROUP OF 3 CHANNELS, EVEN THOUGH THE USER INTERFACE ONLY DISPLAYS A SINGLE CHANNEL. THE RESPECTIVE TYPES ARE 15, 19, AND 20.
MAPPED CHANNEL	2	BINARY	INDEX OF THE CHANNEL THIS CHANNEL IS MAPPED TO. IF THE CHANNEL IS NOT MAPPED, THE INDEX IS -1.
*ENABLED	1	ASCII	"Y" OR "N"
ACTUAL RATE	4	BINARY	1
SAMPLES PER FRAME	4	BINARY	1
RESERVED	4	N/A	N/A
*BITS PER WORD	2	BINARY	24 FOR CHANNEL TYPE 15 24 FOR CHANNEL TYPE 19 16 FOR CHANNEL TYPE 20
RESERVED	4	N/A	N/A
*CHANNEL NUMBER	2	BINARY	0 FOR CHANNEL TYPE 15 1 FOR CHANNEL TYPE 19 2 FOR CHANNEL TYPE 20
*MODULE ID	1	BINARY	MODULE ID = HEX B1
RESERVED	1	N/A	N/A
*REQUEST SAMPLE RATE	4	BINARY	1
*BITS PER SAMPLE	2	BINARY	24 FOR CHANNEL TYPE 15 24 FOR CHANNEL TYPE 19 16 FOR CHANNEL TYPE 20
DESCRIPTION	20	ASCII	CHANNEL DESCRIPTION
RESERVED	4	N/A	N/A
TCI MODE	1	BINARY	0-GENERATE TIME 1-USE EXTERNAL IRIG SOURCE
RESERVED	3	N/A	N/A

TABLE L-11. TIME CODE OUTPUT CHANNELS			
FIELD	**BYTES**	**FORMAT**	**DESCRIPTION**
CHANNEL TYPE	2	BINARY	TIME CODE MUST APPEAR AS A GROUP OF 3 CHANNELS, EVEN THOUGH THE USER INTERFACE ONLY DISPLAYS A SINGLE CHANNEL. THE RESPECTIVE TYPES ARE 17, 21 AND 22.
MAPPED CHANNEL	2	BINARY	INDEX OF THE CHANNEL THIS CHANNEL IS MAPPED TO. IF THE CHANNEL IS NOT MAPPED, THE INDEX IS -1.
ENABLED	1	ASCII	"Y" - ENABLED, OR "N" - DISABLED
ACTUAL RATE	4	BINARY	1
SAMPLES PER FRAME	4	BINARY	1
RESERVED	4	N/A	N/A
BITS PER WORD	2	BINARY	24 FOR CHANNEL TYPE 17 24 FOR CHANNEL TYPE 21 16 FOR CHANNEL TYPE 22
RESERVED	4	N/A	N/A
CHANNEL NUMBER	2	BINARY	0 FOR CHANNEL TYPE 17 1 FOR CHANNEL TYPE 21 2 FOR CHANNEL TYPE 22
MODULE ID	1	BINARY	MODULE ID = HEX B1
RESERVED	1	N/A	N/A
REQUESTED SAMPLE RATE	4	BINARY	1
BITS PER SAMPLE	2	BINARY	24 FOR CHANNEL TYPE 17 24 FOR CHANNEL TYPE 21 16 FOR CHANNEL TYPE 22
DESCRIPTION	20	ASCII	CHANNEL DESCRIPTION
RESERVED	4	N/A	N/A
TCO MODE	1	BINARY	0 - GENERATE TIME 1 - USE TIME FROM RECORDED TAPE
RESERVED	3	N/A	N/A

TABLE L-12. VOICE INPUT CHANNEL			
FIELD	**BYTES**	**FORMAT**	**DESCRIPTION**
*CHANNEL TYPE	2	BINARY	16
MAPPED CHANNEL	2	BINARY	INDEX OF THE CHANNEL THIS CHANNEL IS MAPPED TO. IF THE CHANNEL IS NOT MAPPED, THE INDEX IS -1.
*ENABLED	1	ASCII	“Y” - ENABLED, OR “N” - DISABLED
ACTUAL RATE	4	BINARY	ACTUAL SAMPLE RATE IN SAMPLES PER SECOND
SAMPLES PER FRAME	4	BINARY	NUMBER OF SAMPLES PER FRAME
RESERVED	4	N/A	N/A
*BITS PER WORD	2	BINARY	8
RESERVED	4	N/A	N/A
*CHANNEL NUMBER	2	BINARY	3
*MODULE ID	1	BINARY	MODULE ID = HEX B1
RESERVED	1	N/A	N/A
*REQUESTED SAMPLE RATE	4	BINARY	2K, 5K, 10K, 20K, 50K, OR 100K
*BITS PER SAMPLE	2	BINARY	8
DESCRIPTION	20	ASCII	CHANNEL DESCRIPTION
RESERVED	1	N/A	N/A
VOLTAGE GAIN	2	BINARY	0 - GAIN OF 1 1 - GAIN OF 2 2 - GAIN OF 4 3 - GAIN OF 8
RESERVED	5	N/A	N/A

TABLE L-13. VOICE OUTPUT CHANNELS			
FIELD	**BYTES**	**FORMAT**	**DESCRIPTION**
CHANNEL TYPE	2	BINARY	18
MAPPED CHANNEL	2	BINARY	INDEX OF THE CHANNEL THIS CHANNEL IS MAPPED TO. IF THE CHANNEL IS NOT MAPPED, THE INDEX IS -1
ENABLED	1	ASCII	"Y" - ENABLED, OR "N" - DISABLED
ACTUAL RATE	4	BINARY	ACTUAL SAMPLE RATE IN SAMPLES PER SECOND
SAMPLES PER FRAME	4	BINARY	NUMBER OF SAMPLES PER FRAME
RESERVED	4	N/A	N/A
BITS PER WORD	2	BINARY	8
RESERVED	4	N/A	N/A
CHANNEL NUMBER	2	BINARY	3
MODULE ID	1	BINARY	MODULE ID = HEX B1
RESERVED	1	N/A	N/A
REQUEST SAMPLE RATE	4	BINARY	NUMBER OF SAMPLES PER SECOND
BITS PER SAMPLE	2	BINARY	8
DESCRIPTION	20	ASCII	CHANNEL DESCRIPTION
RESERVED	8	N/A	N/A

TABLE L-14. BIT SYNC INPUT CHANNELS			
FIELD	**BYTES**	**FORMAT**	**DESCRIPTION**
CHANNEL TYPE	2	BINARY	23
RESERVED	2	N/A	N/A
ENABLED	1	ASCII	“Y” - ENABLED, OR “N” - DISABLED
ACTUAL RATE	4	BINARY	ACTUAL WORD RATE IN WORDS PER SECOND
WORDS PER FRAME	4	BINARY	NUMBER OR WORDS PER FRAME
RESERVED	4	N/A	N/A
BITS PER WORD	2	BINARY	16
RESERVED	4	N/A	N/A
CHANNEL NUMBER	2	BINARY	CHANNEL ON MODULE (0-3)
MODULE ID	1	BINARY	MODULE ID = HEXADECIMAL 13
RESERVED	1	N/A	N/A
REQUESTED RATE	4	BINARY	BITS PER SECOND
DESCRIPTION	20	ASCII	CHANNEL DESCRIPTION
INSTALLED	1	BINARY	0 - DAUGHTER BOARD NOT INSTALLED 1 - DAUGHTER BOARD INSTALLED
PCM GEOG. ADDRESS	1	BINARY	GEOGRAPHICAL ADDRESS OF THE ASSOCIATED PCM INPUT CHANNEL
SOURCE CLOCK	1	BINARY	0 - SOURCE A 1 - SOURCE B
RESERVED	7	N/A	N/A

2.3 Trailer Section. The trailer section contains the setup description and the checksum (see Tables L-15). Early versions of the setup do not contain this information. The “Setup Keys” field in the header indicates the content of the trailer section.

TABLE L-15. TRAILER SECTION FORMAT			
FIELD	**BYTES**	**FORMAT**	**DESCRIPTION**
SETUP DESCRIPTION	40	ASCII	DESCRIPTION OF THE SETUP
SAVED SCANLIST	VARIES	BINARY	NUMBER OF BYTES DEPENDS ON THE NUMBER OF CHANNELS BEING RECORDED.
CHECKSUM	4	BINARY	SUM OF ALL SETUP BYTES.

2.4 Saved Scan-list Structure. This is an array of enabled input channels that make up the calculated scan-list. Each element of the array is made up of two fields, an index field and a count field. The length of the index fields is one byte, and the length of the count field is two bytes.

The index field, which is 1-based, is determined by the position of the channel's module in the ARMOR system. The first input channel found in the ARMOR system is assigned an index of 1, the next input channel is assigned a 2, and so on. The search for input modules starts at slot 1. Filler bytes are assigned an index value of 255.

The count field is the number of words/samples per frame that is assigned to that input channel.

2.5 Creating a Setup Block. Creating a Setup Block involves two steps. In the first step, the user creates an "input" setup block file as described below in this section. Most of the fields in the input setup block file are unspecified (filled with zeros). In the second step, the input setup block file is read by the ARMOR Compiler program that produces a new setup block file with all the unspecified fields initialized to the appropriate values. In other words, a setup block has two types of fields, user specified and compiler generated. Note that all compiler generated fields must be provided in the input setup block file and initialized with zeros prior to executing the ARMOR compiler program.

The rules presented in this section must be explicitly followed to create an ARMOR input setup block. Values for fields identified in the previous tables with an asterisk preceding the field name must be provided. In some cases the values for these required fields are constant and are specified in the tables above. In other cases, the user must provide the desired value. All fields with names not identified with asterisks must be initialized to binary zero. This includes both "unused" and "reserved" fields.

Only input channel information entries are required. Output channel information entries are ignored by the ARMOR Compiler program.

2.5.1 Header Section.

Setup Length	Count the total numbers of bytes in the created setup block and put the value here.
Setup Keys	Set bit 0 = 1 if the trailer contains a description. Leave other bits = 0.
Input Count	Enter the total number of input channel information entries, including both enabled and disabled entries.

2.5.2 Channel Section. PCM, Low Frequency (LF) Analog, and parallel input channel information entries must be included in the setup block in groups of four entries per type. High Frequency (HF) analog input channel information entries must be included in the setup block in groups of two entries per type. Time code /voice input channel information entries must be included in groups of three time code entries and one voice entry. Specifying an ASCII "N" in the enabled field must disable all unused input channel information entries. For each channel information entry group, the channel number field of the first entry in the group is 0 (zero), the second entry is 1, the third is 2, and the fourth is 3. For the time code /voice group, the time code entry channel number fields are 0, 1, and 2 respectively, while the voice entry channel number field is 3. HF analog entry channel number fields are 0 and 1 respectively.

Description fields are not required and are not specified below. However, it is advisable to include an ASCII description of each channel for future reference.

2.5.2.1 PCM Input Channels.

Channel Type	Binary 8
Enabled	ASCII "Y" if enabled, "N" if disabled
Channel Number binary	0,1,2, or 3 as described in 2.5.2 above
Module ID	Hexadecimal 11
Requested Rate	Binary integer rate in bits per second

2.5.2.2 Analog Input Channels.

Channel Type	Binary 5 for LF (up to 1 Megasample /sec), 6 for HF (up to 10 Megasamples/sec)
Enabled	"Y" if enabled, "N" if disabled
Bits per Sample	8 or 12
Channel Number	0,1,2, or 3 as described in 2.5.2 above
Module ID	Hexadecimal 34 (LF) or 33 (HF)
Requested Rate	Binary integer 2K, 5K, 10K, 20K, 50K, 100K, 200K, 500K, 1M (LF, HF) 2.5M, 5M, 10M (HF only)

2.5.2.3 Parallel Input Channels.

Channel Type	Decimal 13
Enabled	"Y" if enabled, "N" if disabled
Channel Number	0,1,2, or 3 as described in 2.5.2 above
Module ID	Hexadecimal 92
Requested Rate	Binary integer 8-bit words (bytes) per second

2.5.2.4 Time Code Input Channels.

Channel Type	Deciaml 15 (1st entry) , 19 (2nd entry), 20 (3rd entry)
Enabled	"Y" if enabled, "N" if disabled, all three entries must be the same
Bits per Word	Deciaml 24 (1st entry), 24 (2nd entry), 16 (3rd entry)
Channel Number	0,1, or 2 as described in 2.5.2 above
Module ID	Hexadecimal B1
Requested Sample Rate	1
Bits per Sample	Decimal 24 (1st entry), 24 (2nd entry), 16 (3rd entry)

2.5.2.5 Voice Input Channels.

Channel Type	Decimal 16
Enabled	"Y" if enabled, "N" if disabled
Bits per Word	8
Channel Number	3 as described in 2.5.2 above
Requested Sample Rate	Integer 2K, 5K, 10K, 50K, 100K
Bits per sample	8

2.5.3 Trailer Section. The trailer section of the input setup block is not required. The user may include an ASCII text setup description in the trailer section by setting the setup keys bit 0 = 1 in the header section (see Section 2.5.1 above) and adding the setup description field only in the trailer section.

2.5.4 ARMOR Compiler Program. Operational instructions for the ARMOR compiler program are provided in the readme.txt file provided with the compiler (see Section 6.17.3.1).